SUPPLEMENT

TO BRITISH TELECOMMUNICATIONS ENGINEERING

(formerly the Supplement to The Post Office Electrical Engineers' Journal)

Vol. 3 Part 3 October 1984

ISSN 0262-4028

BTEC & SCOTEC
GUIDANCE FOR STUDENTS

EDUCATIONAL PAPER

Contents

MICROCOMPUTER SYSTEMS (PART 1)

BUSINESS AND TECHNICIAN EDUCATION COUNCIL

Certificate Programme in Telecommuncations

Sets of model questions and answers for Business and Technician Education Council (BTEC) units are given below. The questions illustrate the types of questions that students may encounter, and are useful as practice material for the skills learned during the course.

Where additional text is given for educational purposes, it is shown within square brackets to distinguish it from information expected of students under examination conditions. Representative time limits are shown for each question, and care has been taken to give model answers that reflect these limits.

We would like to emphasise that the questions are not representative of questions set by any particular college.

BTEC: ELECTRICAL AND ELECTRONIC PRINCIPLES III

The questions in this paper are based on the following sections of the BTEC's standard syllabus U81/742: circuit theorems; alternating-current circuits; DC transients; machines; measuring instruments and measurements; thyristors, diacs, triacs and unijunction transistors. Students are advised to read the notes above

The time for the questions in Section A is one hour, and the time for each question in Section B is 30 min.

SECTION A

Q1 Determine, by using Thévènin's theorem, the voltage across the capacitive reactance in the circuit shown in Fig. 1, if the voltage generator has negligible internal impedance.

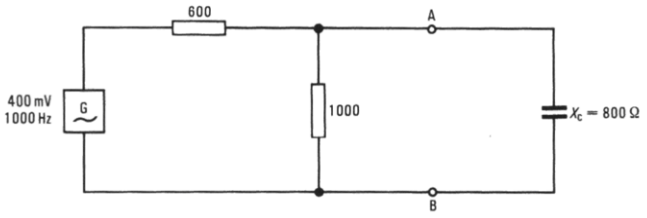


Fig. 1

A1 With reactance X_c disconnected, the voltage across terminals A and B

$$= \frac{1000}{1000 + 600} \times 400 \text{ mV} = \frac{1000 \times 400}{1600} \text{ mV} = 250 \text{ mV}.$$

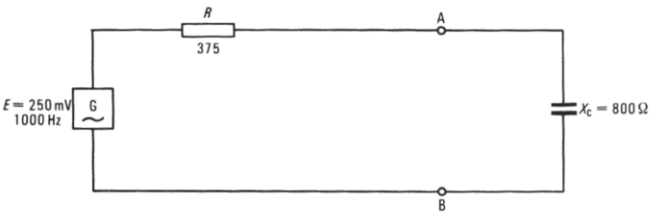
With reactance X_c disconnected and the generator replaced by a short circuit, the resistance across AB is

$$R_{AB} = \frac{600 \times 1000}{600 + 1000} \Omega = \frac{600 \times 1000}{1600} \Omega = 375 \Omega.$$

[*Tutorial note:* The short circuit represents the negligible impedance of the generator.]

The initial circuit is now simplified to the circuit shown in sketch (*a*). The total impedance, Z, is given by

$$Z = \sqrt{(R^2 + X_c^2)} = \sqrt{(375^2 + 800^2)} \Omega = 883{\cdot}5 \Omega.$$



(*a*)

The current, $I = \frac{E}{Z} = \frac{250 \times 10^{-3}}{883{\cdot}5}$ A.

The voltage across reactance X_c

$$= IX_c = \frac{250 \times 10^{-3}}{883{\cdot}5} \times 800 \text{ V} = \underline{226{\cdot}4 \text{ mV}}.$$

Q2 Calculate the maximum power that can be dissipated in the variable resistor R_L in the circuit shown in Fig. 2, if the 12 V battery has an internal resistance of 1 Ω.

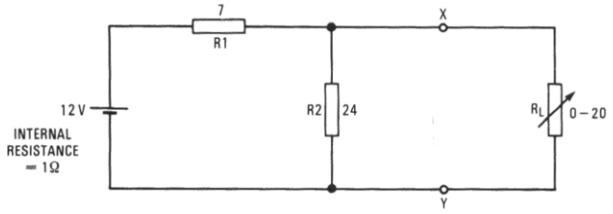


Fig. 2

A2 Maximum power is dissipated when the value of resistor R_L is equal to the internal resistance of the network comprising resistors R1 and R2, and the 12 V battery.

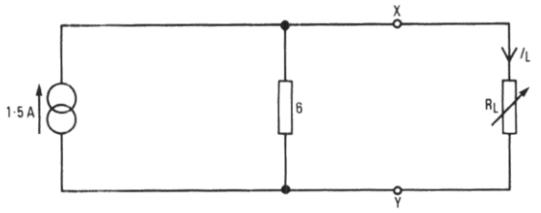
One method of simplifying this network is by using Norton's theorem. The current flowing between terminals X and Y when they are short-circuited is given by

$$I_{sc} = \frac{12}{1+7}\text{ A} = 1{\cdot}5\text{ A}.$$

With resistor R_L disconnected and the battery replaced by a 1 Ω resistance, the resistance across terminals X and Y is given by

$$R_{XY} = \frac{(1+7)\times 24}{(1+7)+24}\,\Omega = \frac{8\times 24}{32}\,\Omega = 6\,\Omega.$$

The simplified network and load R_L are shown in the sketch.



Maximum power is dissipated in resistor R_L when R_L equals 6 Ω. Therefore, the current through resistor R_L

$$= \frac{1{\cdot}5}{2}\text{ A} = 0{\cdot}75\text{ A}.$$

Therefore, the maximum power dissipated

$$= I_L^2 \times R_L = 0{\cdot}75^2 \times 6\text{ W} = \underline{3{\cdot}375\text{ W}}.$$

Q3 *A coil is connected in series with a 100 nF capacitor (C) across a variable frequency source, the output of which is kept constant at 4 V. The relationship between the circuit current and the frequency is shown in Fig 3. Determine the inductance, L, and the resistance, R, of the coil.*

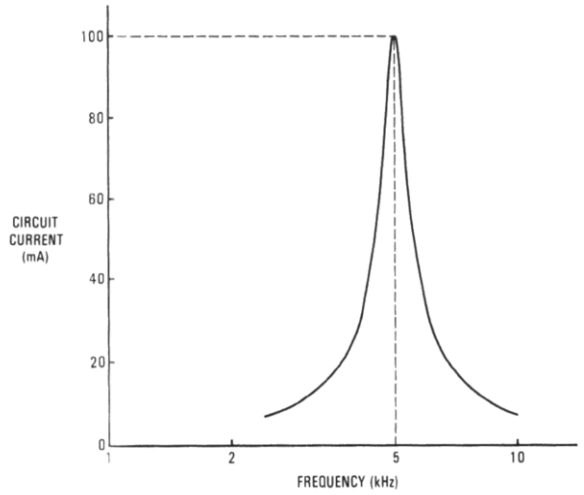


Fig. 3

A3 Maximum current flows when the circuit is at resonance. Therefore, the resonant frequency, $f_0 = 5$ kHz. At resonance, the inductive reactance is equal to the capacitative reactance.

$$\therefore \quad 2\pi f_0 L = \frac{1}{2\pi f_0 C}.$$

$$\therefore \quad L = \frac{1}{(2\pi f_0)^2 C},$$

$$= \frac{1}{(2\pi\times 5\times 10^3)^2 \times 100\times 10^{-9}}\text{ H},$$

$$= \underline{10{\cdot}13\text{ mH}}.$$

At resonance, the total impedance = R.

$$\therefore \quad R = \frac{\text{voltage}}{\text{current}} = \frac{4}{100\times 10^{-3}}\,\Omega = \underline{40\,\Omega}.$$

Q4 *Two identical low-loss parallel tuned circuits, A and B, are coupled by mutual inductance, M, as shown in Fig. 4. When the signal-generator output voltage is maintained constant while the frequency is varied, sketch the variation of the circulating current in circuit B for the following coupling conditions:*

(a) under coupled,
(b) critically coupled, and
(c) over coupled.

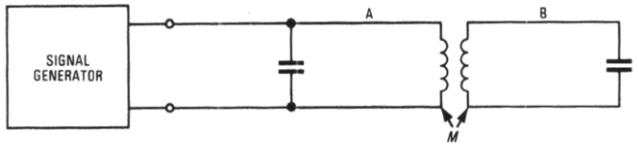
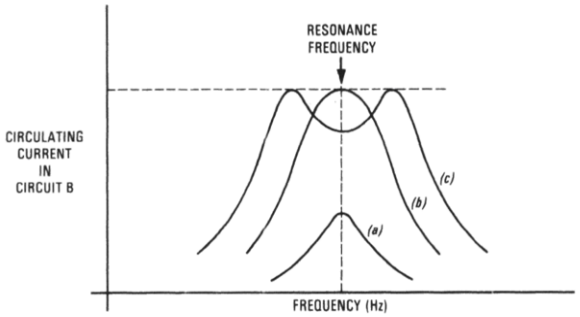


Fig. 4

A4 The response curves for circuit B are shown in the sketch.



[*Tutorial note:* As the coefficient of coupling is increased, the circulating current at resonance increases to a maximum value when the circuits are critically coupled.

The coefficient of critical coupling, $k_c = 1/Q$, where Q = the Q-factor of circuit A = Q-factor of circuit B.

As the coupling is further increased, the response curve displays double humps, the peaks of which become more pronounced and spread further apart. The magnitude of the two peaks is substantially the same as the peak value at critical coupling.]

Q5 *The output voltage of a DC shunt generator is required to remain constant at 200 V. The resistance of the armature winding is 0·25 Ω and the field current remains constant at 2 A. When the load on the generator is 2 kW, the armature rotates at 500 rev/min.*

Assuming that the effect of armature reaction is negligible, determine the required speed of armature rotation to supply a 4 kW load.

A5 2 kW Load

The initial load current, I_{L1}, is given by

$$I_{L1} = \frac{P_1}{V},$$

where P_1 is the initial power and V is the initial voltage.

$$\therefore \quad I_{L1} = \frac{2000}{200} = 10\text{ A}.$$

The initial generated EMF, E_1, is given by

$$E_1 = V + (I_{L1} + I_f)R_a,$$

where I_f is the field current and R_a is the resistance of the armature winding.

$$\therefore \quad E_1 = 200 + (10 + 2) \times 0{\cdot}25 = 203 \text{ V}.$$

4 kW Load

Similarly, the final load current, I_{L2}, is given by

$$I_{L2} = \frac{P_2}{V} = \frac{4000}{200} = 20 \text{ A}.$$

The final generated EMF, E_2, is given by

$$E_2 = V + (I_{L2} + I_f)R_a = 200 + (20 + 2) \times 0{\cdot}25,$$
$$= 205{\cdot}5 \text{ V}.$$

The generated EMF, E, is given by

$$E = kN\Phi,$$

where k is a constant, N is the armature speed and Φ is the flux.

As the flux produced by the shunt field remains constant, $E \propto N$. Therefore, E/N is constant.

$$\therefore \quad \frac{E_1}{N_1} = \frac{E_2}{N_2}.$$

Therefore, the required armature speed, N_2,

$$= \frac{N_1 E_2}{E_1} = \frac{500 \times 205{\cdot}5}{203} \text{ rev/min},$$
$$= \underline{506{\cdot}2 \text{ rev/min.}}$$

Q6 *A simplified diagram of the stator coils of an induction motor is shown in Fig. 5. The waveforms of the stator-coil currents are shown in Fig. 6. When the currents are positive, they flow in the directions indicated in Fig. 5.*

Sketch the individual stator field directions together with the resultant field direction at the instants denoted X, Y and Z in Fig. 6.

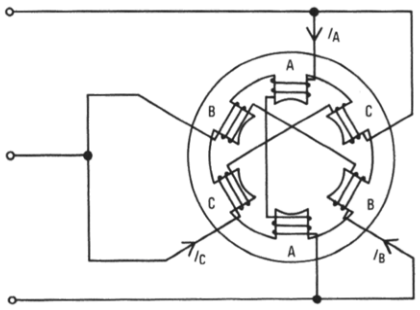


Fig. 5

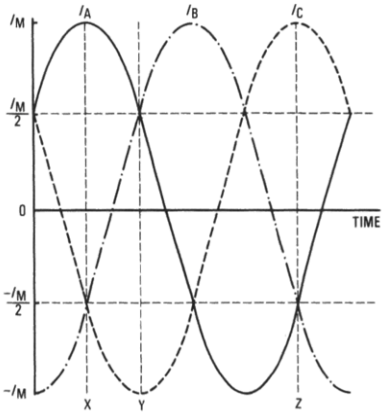
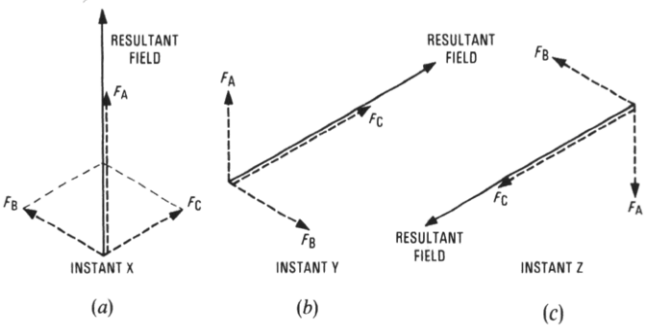


Fig. 6

A6 Stator-coil flux is proportional to stator-coil current. The resultant field directions at instants X, Y and Z are shown in sketches (*a*), (*b*) and (*c*), respectively. F_A, F_B and F_C refer to the fluxes produced by coils A, B and C, respectively.



Q7 *The input circuit of an electronic voltmeter measures the peak value of the input waveform. The instrument is calibrated to read the RMS value of a sinusoidal waveform.*

Determine the percentage error obtained when the instrument is used to measure the waveform shown in Fig. 7.

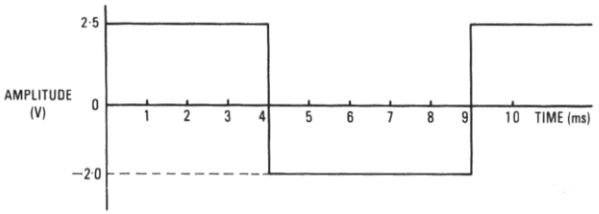
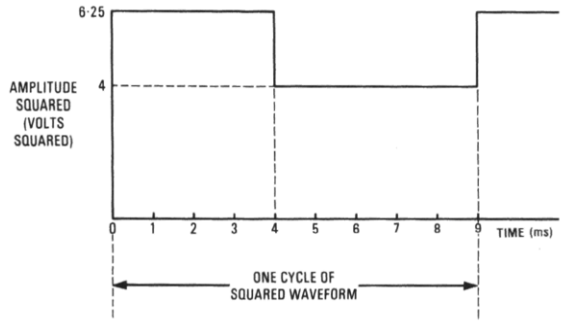


Fig. 7

A7 The peak value of the measured waveform = 2·5 V. The meter reading for the measured waveform

$$= \frac{1}{\sqrt{2}} \times 2{\cdot}5 \text{ V} = 1{\cdot}768 \text{ V}.$$

The squared version of the waveform to be measured is shown in the sketch.



The area enclosed by the squared waveform

$$= (4 \times 6{\cdot}25) + (5 \times 4) \text{ V ms} = 25 + 20 \text{ V ms},$$
$$= 45 \text{ V ms}.$$

The mean square value of the measured waveform

$$= \frac{45}{9} \text{ V} = 5 \text{ V}.$$

Therefore, the root square value of the measured waveform

$$= \sqrt{5} \text{ V} = 2{\cdot}236 \text{ V}.$$

As the meter should read 2·236 V, the error

$$= 2{\cdot}236 - 1{\cdot}768 = 0{\cdot}468 \text{ V},$$

and the percentage error

$$= \frac{0{\cdot}468}{2{\cdot}236} \times 100\% = \underline{20{\cdot}9\%.}$$

Q8 *A multirange meter has a sensitivity of 20 000 Ω/V on its DC-voltage ranges. This meter is used on its 10 V range to measure the potential difference between points A and B in the circuit shown in Fig. 8.*
Calculate the meter reading.

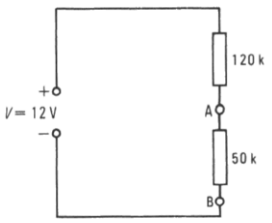


Fig. 8

A8 The resistance of the meter

= full-scale deflection voltage × sensitivity,

$= 10 \times 20\,000\ \Omega = 200\ \text{k}\Omega.$

When the meter is connected for the measurement, the resistance between points A and B is given by

$$R_{AB} = \frac{50 \times 200}{50 + 200}\ \text{k}\Omega = 40\ \text{k}\Omega.$$

Total resistance, R_T,

$$= 120 + 40\ \text{k}\Omega = 160\ \text{k}\Omega.$$

Supply current, I, is given by

$$I = \frac{V}{R_T} = \frac{12}{160 \times 10^3}\ \text{A}.$$

Meter reading = potential difference between A and B,

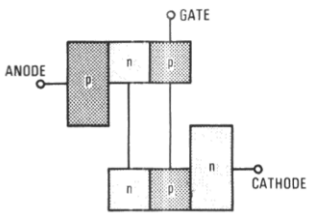
$= IR_{AB}$,

$$= \frac{12}{160 \times 10^3} \times 40 \times 10^3\ \text{V},$$

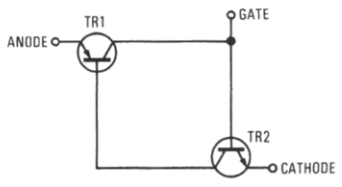
$= \underline{3\ \text{V}}.$

Q9 *Explain briefly how a thyristor may be represented by a two-transistor model.*

A9 A thyristor is basically a four-layer p n p n device having three terminals.
If the inner p and n sections are split and pulled apart, the result is two interconnected complementary transistors, as shown in sketch (*a*). This may be re-drawn to produce the two-transistor model shown in sketch (*b*).



(*a*)



(*b*)

Q10 *Explain briefly the operation of the circuit shown in Fig. 9. Sketch the waveforms expected at points X and Y, together with their time relationships.*

A10 With the unijunction transistor (UJT) in its non-triggered state, a small current flows through the high inter-base resistance of the UJT and R2, and the emitter junction is reverse biased. Capacitor C charges

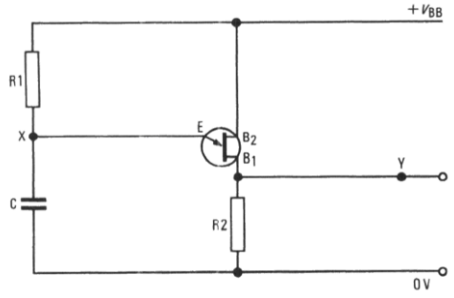
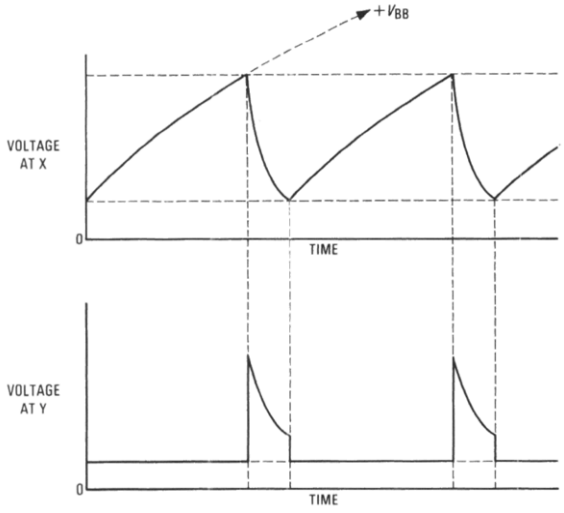


Fig. 9

exponentially through R1 towards the positive supply voltage, V_{BB}. When the potential at point X is sufficiently positive for the emitter junction to become forward biased, the resistance of the n-type silicon between terminals E and B1 falls drastically.

[*Tutorial note:* The substantial reduction in resistance is due to the injection of charge carriers across the forward-biased junction.]

This low resistance provides a discharge path via resistor R2 for the capacitor. The resistance of R2 would generally be considerably less than the resistance of R1, and so the discharge of the capacitor is relatively rapid. The potential at X falls to a point where the emitter junction becomes reverse biased and the UJT reverts to its initial state. The action is then repeated.
The waveforms at points X and Y are shown in the sketch.



SECTION B

Q11 *The data shown in the table was obtained during tests on the circuit shown in Fig. 10.*
If the supply frequency is 400 Hz, and if the meters have a negligible effect on the circuit, calculate

(*a*) *the values of L, C and R, and*
(*b*) *the value of the component required in series with the circuit to produce a power factor of unity.*

V_1	V_2	I	Power Factor
100 V	182·8 V	2·14 A	0·856 lagging

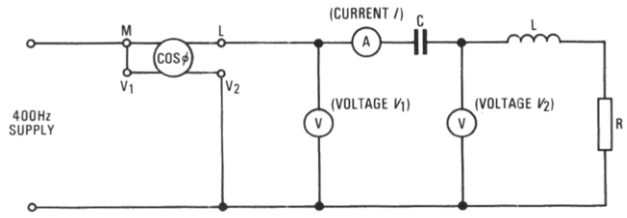


Fig. 10

A11 (*a*) The apparent power = $V_1 I = 214$ V A.

The power factor, $\cos\phi = \dfrac{\text{true power}}{\text{apparent power}}$.

Therefore, the true power

$$= V_1 I \cos\phi = 214 \times 0{\cdot}856 \text{ W} = 183{\cdot}18 \text{ W}.$$

The true power = I^2R.

$$\therefore \quad R = \frac{\text{true power}}{I^2} = \frac{183{\cdot}18}{(2{\cdot}14)^2}\ \Omega = \underline{40\ \Omega.}$$

The total impedance of L and R is given by

$$Z_{LR} = \frac{V_2}{I} = \frac{182{\cdot}8}{2{\cdot}14}\ \Omega = 85{\cdot}42\ \Omega.$$

But, $$Z_{LR} = \sqrt{(R^2 + X_L^2)},$$

where X_L is the reactance of the inductor L.

$$\therefore \quad Z_{LR}^2 = R^2 + X_L^2.$$

$$\therefore \quad X_L^2 = Z_{LR}^2 - R^2.$$

$$\therefore \quad X_L = \sqrt{(Z_{LR}^2 - R^2)},$$

$$= \sqrt{(85{\cdot}42^2 - 40^2)},$$

$$= 75{\cdot}48\ \Omega.$$

At frequency f, $X_L = 2\pi fL$.

$$\therefore \quad L = \frac{X_L}{2\pi f} = \frac{75{\cdot}48}{800\pi} = \underline{30 \text{ mH.}}$$

The total impedance, Z_T,

$$= \frac{V_1}{I} = \frac{100}{2{\cdot}14}\ \Omega = 46{\cdot}73\ \Omega.$$

But, $$Z_T = \sqrt{(R^2 + X^2)},$$

where X is the total reactance.

$$\therefore \quad Z_T^2 = R^2 + X^2.$$

$$\therefore \quad X^2 = Z_T^2 - R^2.$$

$$\therefore \quad X = \sqrt{(Z_T^2 - R^2)},$$

$$= \sqrt{(46{\cdot}73^2 - 40^2)},$$

$$= 24{\cdot}16\ \Omega$$

As the power factor is lagging, the current, I, lags the voltage V_1.

$$\therefore \quad X_L > X_C.$$

But, $$X = X_L - X_C.$$

$$\therefore \quad X_C = X_L - X,$$

$$= 75{\cdot}48 - 24{\cdot}16\ \Omega,$$

$$= 51{\cdot}32\ \Omega.$$

But, $$X_C = \frac{1}{2\pi fC}.$$

$$\therefore \quad C = \frac{1}{2\pi f X_C},$$

$$= \frac{1}{800 \times \pi \times 51{\cdot}32}\ \text{F},$$

$$= \underline{7{\cdot}75\ \mu\text{F.}}$$

(*b*) The correction of the power factor to unity requires a total reactance of zero.

Therefore, the new $X_C = X_L = 75{\cdot}48\ \Omega$.

The required value of total capacitance, C_T, is given by

$$C_T = \frac{1}{2\pi f X_C} = \frac{1}{800 \times \pi \times 75{\cdot}48} = 5{\cdot}27\ \mu\text{F}.$$

The reduced capacitance is obtained by connecting an additional capacitor C_A in series with the circuit.

The total capacitance, $C_T = \dfrac{CC_A}{C + C_A}$.

$$\therefore \quad C_T(C + C_A) = CC_A.$$

$$\therefore \quad C_T C + C_T C_A = CC_A.$$

$$\therefore \quad CC_A - C_T C_A = C_T C.$$

$$\therefore \quad C_A(C - C_T) = C_T C.$$

$$\therefore \quad C_A = \frac{C_T C}{C - C_T},$$

$$= \frac{5{\cdot}27 \times 7{\cdot}75}{7{\cdot}75 - 5{\cdot}27}\ \mu\text{F},$$

$$= \underline{16{\cdot}47\ \mu\text{F.}}$$

Q12 *A low-loss parallel tuned circuit is connected in series with a 1·5 kΩ resistor across the output of a signal generator, whose output is maintained constant at 10 V as the frequency is varied. The parallel tuned circuit consists of a coil having an inductance of 10 mH in parallel with a loss-free capacitor. An electronic voltmeter connected across the tuned circuit indicates a maximum reading of 8·5 V when the output frequency of the signal generator is 9·2 kHz.*

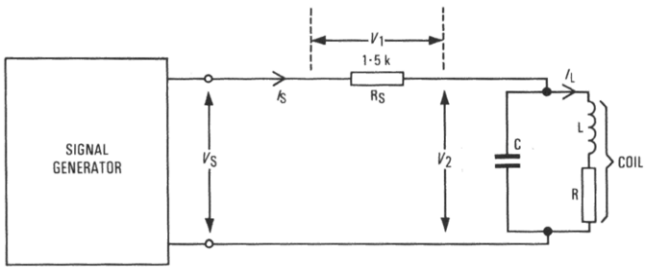
(*a*) *Calculate the following for the parallel tuned circuit:*

(*i*) *the capacitance of the capacitor,*
(*ii*) *the dynamic impedance, and*
(*iii*) *the resistance of the coil.*

(*b*) *If the output frequency of the signal generator is 9·2 kHz, determine*

(*i*) *the power dissipated in the tuned circuit, and*
(*ii*) *the current flowing through the coil.*

A12 The sketch shows the complete circuit.



(*a*) (*i*) The tuned circuit resonates at 9·2 kHz. As the parallel tuned circuit is a low-loss circuit, the resonant frequency, f_0, is given by

$$f_0 = \frac{1}{2\pi\sqrt{(LC)}}.$$

$$\therefore \quad 2\pi f_0 = \frac{1}{\sqrt{(LC)}}.$$

$$\therefore \quad (2\pi f_0)^2 = \frac{1}{LC}.$$

$$\therefore \quad C = \frac{1}{(2\pi f_0)^2 L},$$

$$= \frac{1}{(2\pi \times 9{\cdot}2 \times 10^3)^2 \times 10 \times 10^{-3}}\ \text{F},$$

$$= \underline{29{\cdot}93 \text{ nF.}}$$

(*ii*) At resonance, the voltage, V_2, across the tuned circuit is in phase with the supply current, I_S. Therefore V_2 is in phase with V_1, the voltage across resistor R_S.

Now, $$V_S = V_1 + V_2.$$

$$\therefore \quad V_1 = V_S - V_2 = 10 - 8{\cdot}5 \text{ V} = 1{\cdot}5 \text{ V}.$$

Also, $$I_S = \frac{V_1}{R_S} = \frac{1{\cdot}5}{1{\cdot}5 \times 10^3}\ \text{A} = 1 \text{ mA}.$$

The dynamic impedance, Z_0, of the tuned circuit is given by

$$Z_0 = \frac{V_2}{I_S} = \frac{8{\cdot}5}{1 \times 10^{-3}}\ \Omega = 8{\cdot}5\ \text{k}\Omega.$$

(*iii*) The dynamic impedance, $Z_0 = \dfrac{L}{CR}$.

$$\therefore \quad R = \frac{L}{CZ_0} = \frac{10 \times 10^{-3}}{29{\cdot}93 \times 10^{-9} \times 8{\cdot}5 \times 10^{3}}\ \Omega,$$

$$= \underline{39{\cdot}31\ \Omega.}$$

(*b*) (*i*) The power dissipated is the product of the in-phase components of voltage and current. As V_2 and I_S are in phase when the frequency is 9·2 kHz, the power dissipated in the tuned circuit, P,

$$= V_2 I_S = 8{\cdot}5 \times 1 \times 10^{-3}\ \text{W} = \underline{8{\cdot}5\ \text{mW.}}$$

(*ii*) The only power dissipated, P, in the tuned circuit, is due to the current I_L flowing through the resistance, R, of the coil.

$$\therefore \quad P = I_L^2 R.$$

$$\therefore \quad I_L^2 = \frac{P}{R}.$$

$$I_L = \sqrt{\left(\frac{P}{R}\right)},$$

$$= \sqrt{\left(\frac{8{\cdot}5 \times 10^{-3}}{39{\cdot}31}\right)}\ \text{A},$$

$$= \underline{14{\cdot}7\ \text{mA.}}$$

Q13 (*a*) *Explain, with the aid of a sketch, the significance of the 'time constant' of a series CR circuit.*

(*b*) *The capacitor shown in Fig. 11 is initially discharged. The ammeter indicates a reading of 2 mA at the instant switch S is closed. Once the capacitor is fully charged, the ammeter reads 0·8 mA.*

If the time constant of the discharge circuit is 3·6 s, calculate

(*i*) *the capacitance of the capacitor,*

(*ii*) *the energy stored by the capacitor when it is fully charged, and*

(*iii*) *the charge held by the capacitor 5 s after opening switch S (assume that the capacitor was fully charged before the switch was opened).*

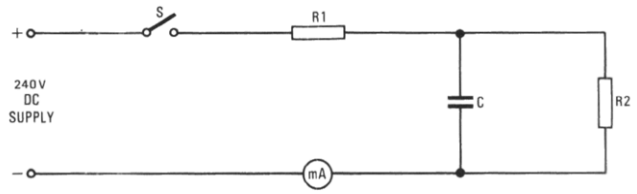
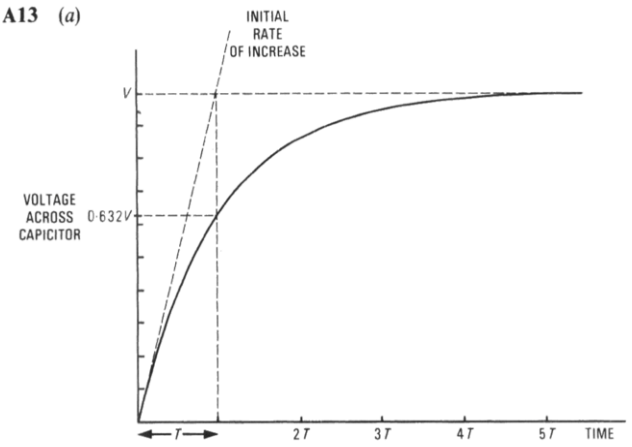


Fig. 11

A13 (*a*)



The sketch shows the variation of voltage across a capacitor when it is charged from a DC supply of V volts through a resistance R. The time constant, T, shown in the sketch is the time taken for the voltage across the capacitor to reach 63·2% of the applied voltage. It is also the time taken to fully charge the capacitor if the initial rate of voltage increase is maintained.

The time constant, $T = CR$ seconds.

During discharge, the capacitor voltage falls to 36·8% of its initial value in a time equal to the time constant.

(*b*) (*i*) At the instant switch S is closed, the charge held by the capacitor = 0 coulombs.

Therefore, the potential difference across the capacitor = 0 V, and the potential difference across resistor R1 = 240 V.

$$\therefore \quad R_1 = \frac{240}{2 \times 10^{-3}}\ \Omega = 120\ \text{k}\Omega.$$

When the capacitor is fully charged, no current flows in the capacitive branch; that is, capacitor C behaves as an open circuit.

The total resistance of the circuit, R_T,

$$= \frac{240}{0{\cdot}8 \times 10^{-3}}\ \Omega = 300\ \text{k}\Omega.$$

$$\therefore \quad R_2 = R_T - R_1 = 300 - 120\ \text{k}\Omega = 180\ \text{k}\Omega.$$

The time constant of the discharge circuit, T, $= CR_2$.

$$\therefore \quad C = \frac{T}{R_2} = \frac{3{\cdot}6}{180 \times 10^{3}}\ \text{F} = \underline{20\ \mu\text{F.}}$$

(*ii*) When the capacitor is fully charged, the potential difference across the capacitor

= the potential difference across R2,

$$= 0{\cdot}8 \times 10^{-3} \times 180 \times 10^{3}\ \text{V}$$

$$= 144\ \text{V}.$$

The energy stored by the capacitor

$$= \tfrac{1}{2}CV^2 = \tfrac{1}{2} \times 20 \times 10^{-6} \times (144)^2\ \text{J} = \underline{0{\cdot}207\ \text{J.}}$$

(*iii*) The potential difference across the capacitor, v_c, during discharge is given by

$$v_c = Ve^{-t/CR}$$

The potential difference at commencement of discharge, $V = 144$ V.

After 5 s, $v_c = 144e^{-5/3{\cdot}6} = 35{\cdot}91$ V.

The charge held by the capacitor

$$= Cv_c = 20 \times 10^{-6} \times 35{\cdot}91\ \text{coulombs} = \underline{718{\cdot}2\ \mu\text{C.}}$$

Q14 (*a*) *Explain, with the aid of a circuit diagram, the need for a starter with a DC motor.*

(*b*) *A 240 V series motor requires a current of 18 A to produce a torque of 40 N m at a shaft speed of 800 rev/min. The load on the motor is increased to 110 N m.*

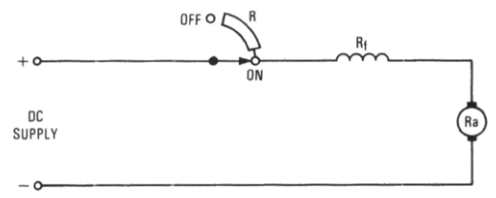
Calculate for the increased load:

(*i*) *the supply current,*

(*ii*) *the shaft speed if the combined resistance of the armature winding and the series field is 0·7 Ω.*

A14 (*a*) When a DC motor is running, an EMF is induced in the rotating armature which opposes the applied voltage (Lenz's law). The induced EMF limits the current flowing through the motor. When the armature is stationary, no induced EMF is present. The only opposition to current flow is provided by the combined resistance of the armature and the field winding. This would give rise to a very large current when the motor is initially started, because of the low value of the combined armature and field winding resistance.

The function of the starter is to limit the initial starting current by connecting resistance in series with the armature. This is the resistance R in the sketch. As the motor speed increases so does the EMF induced



in the armature; thus, the series resistance can be reduced until it is finally cut out completely. This is the condition shown in the sketch.

(*b*) (*i*) The motor torque, $T \propto \Phi I_a$, where Φ is the flux produced by the field winding, and I_a is the armature current.

In a series motor,

$$\Phi \propto I_a.$$

$$\therefore \quad T \propto I_a^2.$$

$$\therefore \quad \frac{T}{I_a^2} = \text{constant}.$$

In the initial condition, $T_1 = 40$ N m and $I_{a1} = 18$ A.
The new torque, T_2, $= 110$ N m.
The required supply current = armature current, I_{a2} (series motor).

Now,
$$\frac{T_2}{(I_{a2})^2} = \frac{T_1}{(I_{a1})^2}.$$

$$\therefore \quad (I_{a2})^2 = \frac{(I_{a1})^2 T_2}{T_1}.$$

$$\therefore \quad I_{a2} = \sqrt{\left\{\frac{(I_a)^2 T_2}{T_1}\right\}},$$

$$= \sqrt{\left\{\frac{(18)^2 \times 110}{40}\right\}},$$

$$= \underline{29{\cdot}85 \text{ A.}}$$

(*ii*) The supply voltage, V, is given by

$$V = E + I_a(R_a + R_f),$$

where E is the EMF induced in the armature, and $(R_a + R_f)$ is the combined resistance of the armature and field.

With the initial load, $T_1 = 40$ N m and $I_{a1} = 18$ A.

$$\therefore \quad 240 = E_1 + (18 \times 0{\cdot}7).$$

$$\therefore \quad E_1 = 240 - (18 \times 0{\cdot}7),$$

$$= 227{\cdot}4 \text{ V}.$$

With the new load, $T_2 = 110$ N m and $I_{a2} = 29{\cdot}85$ A.

$$\therefore \quad E_2 = 240 - (29{\cdot}85 \times 0{\cdot}7),$$

$$= 219{\cdot}1 \text{ V}.$$

Now,
$$E \propto N\Phi,$$

where N is the motor speed, and Φ is the field flux.

In a series motor, $\Phi \propto I_a$.

$$\therefore \quad E \propto NI_a.$$

$$\therefore \quad \frac{E}{NI_a} = \text{constant}.$$

The values for this formula are summarised in the following table

Initial condition	New condition
$E_1 = 227{\cdot}4$ V	$E_2 = 219{\cdot}1$ V
$I_{a1} = 18$ A	$I_{a2} = 29{\cdot}85$ A
$N_1 = 800$ rev/min	N_2

$$\frac{E_1}{N_1 I_{a1}} = \frac{E_2}{N_2 I_{a2}}.$$

$$\therefore \quad N_2 = \frac{N_1 I_{a1} E_2}{E_1 I_{a2}},$$

$$= \frac{800 \times 18 \times 219{\cdot}1}{227{\cdot}4 \times 29{\cdot}85} \text{ rev/min},$$

$$\therefore \quad = \underline{464{\cdot}8 \text{ rev/min.}}$$

Questions and answers contributed by C. Wright

BTEC: TELEPHONE SWITCHING SYSTEMS III

The following questions are based on the BTEC's standard unit U81/745. Students are advised to read the notes on p. 49

Q1 *If the traffic flow in erlangs during a specified period is known, state three items of information that can be derived from this knowledge.* (*4 min*)

A1 (*a*) The average number of simultaneous calls during the specified period.
(*b*) The portion of the specified period for which a circuit is engaged.
(*c*) The number of calls which originate during a period equal to the average holding time of the calls occurring in the specified period.

Q2 *The number of calls carried by a rank of exchange switches are counted at intervals of 10 min during a 1 h period. The number of simultaneous calls in progress at each count were 20, 28, 16, 23, 22, 18, 20.*
Find the traffic intensity. (*4 min*)

A2 From Q1, the traffic intensity is given by the average number of simultaneous calls in progress during the 1 h period.
The average number of simultaneous calls in progress is given by

$$\frac{20 + 28 + 16 + 23 + 22 + 18 + 20}{7} = \frac{147}{7} = 21.$$

Therefore, the traffic intensity $= \underline{21 \text{ erlangs.}}$

Q3 *Distinguish between pure-chance and smooth traffic.* (*4 min*)

A3 Pure-chance traffic may occur at any time of day or night and for any reason. It is traffic in which a call is as likely to originate at any one moment as at any other.
Smooth traffic is traffic which does not, at any time, differ greatly from the average traffic measured over a period of time.

Q4 *If each circuit in a 4-circuit group has a probability of being engaged of 0·4, what is the probability of circuits 1 and 2 being engaged and circuits 3 and 4 being free?* (*3 min*)

A4 If the probability of a circuit being engaged is 0·4, then the probability that it is free is 0·6.
Therefore, the probability of circuits 1 and 2 being engaged

$$= 0{\cdot}4 \times 0{\cdot}4 = 0{\cdot}16.$$

The probability of circuits 3 and 4 being free

$$= 0{\cdot}6 \times 0{\cdot}6 = 0{\cdot}36.$$

Hence, the probability of circuits 1 and 2 being engaged, and circuits 3 and 4 being free

$$= 0{\cdot}16 \times 0{\cdot}36 = \underline{0{\cdot}0576.}$$

Q5 In a single queue, the probability of a call having to wait is the product of the number of calls arriving in a specific period and the mean holding time of the calls. *TRUE/FALSE* (*1 min*)

A5 False. [*Tutorial note:* The waiting probability is the product of the number of calls and the mean holding time of the server.]

Q6 The average time spent in a single queue system is

(*a*) $\frac{A}{1-H}$,

(*b*) $\frac{H}{1-A}$,

(*c*) $\frac{1}{1-A}$,

(*d*) $\frac{A}{1-A}$, *or*

(*e*) $\frac{1-A}{H}$,

where A is the traffic intensity and H is the mean holding time of the server. (*2 min*)

A6 (*b*) $\frac{H}{1-A}$

Q7 For each of the requirements listed below, state whether in-band or out-band signalling would be used:

(*a*) *Signalling to take place during speech transmission.*
(*b*) *Uses standard transmission terminal equipment.*
(*c*) *Uses the simplest form of signal-detection circuit.* (*3 min*)

A7 (*a*) Out-band
(*b*) In-band
(*c*) Out-band

Q8 SSAC9 signalling is most commonly used

(*a*) *between MSCs on the transit network,*
(*b*) *on STD calls between GSCs,*
(*c*) *between directly-connected DSCs on the transit network,*
(*d*) *on links between crossbar exchanges, or*
(*e*) *between local exchanges and parent GSCs.*

Choose an option. (*2 min*)

A8 (*b*) on STD calls between GSCs.
[*Tutorial note:* SSAC9 signalling is not used at all in the transit network, SSAC11 and SSMF2 being the most commonly used systems. Also, SSAC9 will only be used on the GSC network when either line or system conditions prevent the use of similar and cheaper alternatives; for example, loop-disconnect signalling, SSDC2 signalling.]

Q9 The following questions refer to Fig. 1, which shows a 2-link transit-connected call. Assume that a calling subscriber dials 083350099.

(*a*) *Which digits are stored in the controlling register?*
(*b*) *What information is provided by the controlling register?*
(*c*) *Which digits are transferred to the TSC register?*
(*d*) *What type of signalling system is most commonly used for the digit transfer in part* (*c*)*?*
(*e*) *Is the AC11 line signalling system a tone-on idle or a tone-off idle system?*
(*f*) *When does the TSC register release?*
(*g*) *After the interchange of forward and backward prefixes between the controlling and terminal GSCs, what is the first MF signal returned by the terminal GSC?*
(*h*) *Which digits are transmitted to the terminal GSC?* (*10 min*)

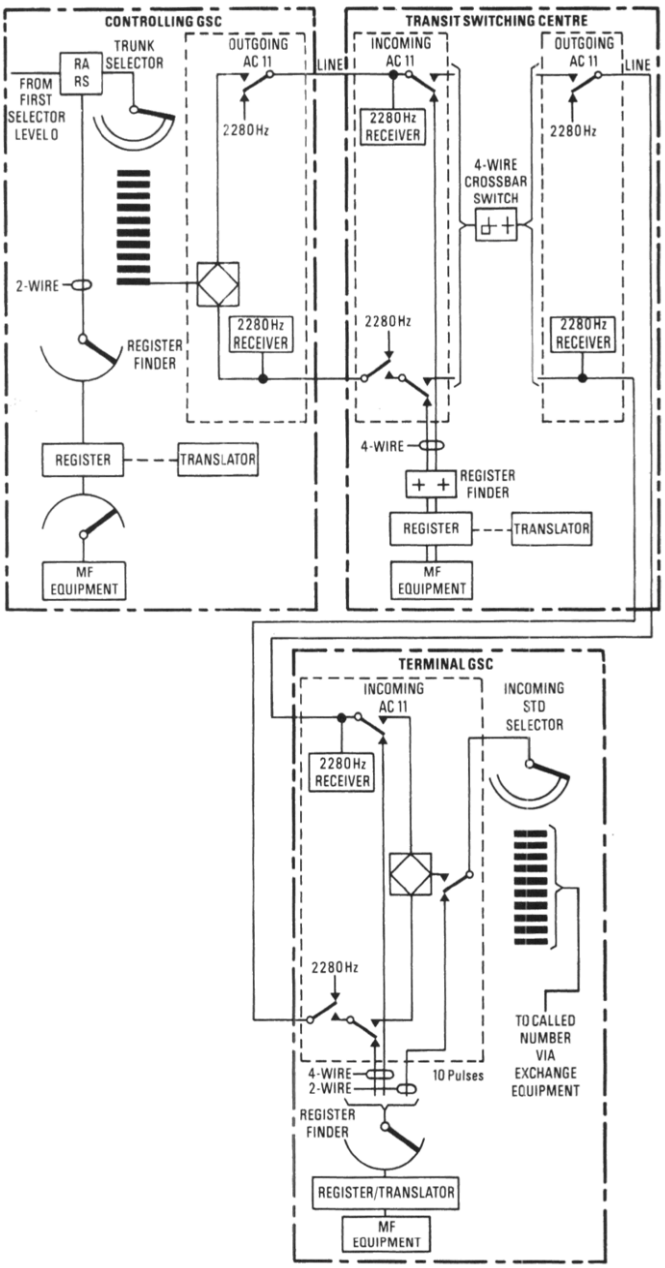


Fig. 1

A9 (*a*) 83350099.

(*b*) (*i*) Metering rate,
(*ii*) translation digits for routeing to TSC, and
(*iii*) that MF equipment is required.

(*c*) The A, B, and C digits; that is, 833.
(*d*) Signalling system multi-frequency No. 2 (SSMF2).
(*e*) Tone-off idle.
(*f*) After translation of the forwarded ABC digits from the controlling GSC and seizure of the outgoing AC11 relay-set.
(*g*) Terminal proceed to send.
(*h*) The C-digit plus the remaining numerical digits; that is, in this case, 350099.

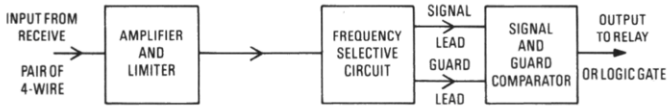
[*Tutorial note:* The transmission of the C-digit is at a terminal GSC which serves more than one charge group where it is used for local translation. If it is not required, it is ignored by the terminal GSC.]

Q10 Explain the function of 'compelled' signals as opposed to 'pulsed' signals. (*5 min*)

A10 Compelled signals are of no fixed duration but persist until acknowledged by the distant end. They are transmitted in both directions prior to any information transmission and serve to verify the continuity of the transmission paths in both directions between the terminal exchanges. After successful exchange of compelled signals, digital information is transmitted in the form of fixed duration (typically 80 ms) coded signals.

Q11 With the aid of a suitable block diagram, explain the functions of an SSAC9 VF receiver. (*10 min*)

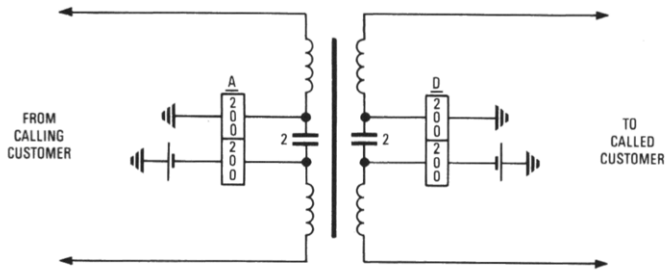
A11 The received signal is brought to a pre-determined level by the amplifier limiter stage in order to make receiver performance independent of signal level. The signal is then fed to a frequency-selective circuit and at 2280 Hz. There will be a maximum output voltage on the signal lead and a minimum output on the guard lead. At all other frequencies,



the guard lead voltage will be relatively high and that on the signal lead will be minimal. The two outputs are then fed to a comparator which compares the values of the signal and guard voltages and produces an output only if the signal voltage is significantly greater than the guard voltage. This output is then used to control the buffer amplifier and apply the appropriate 2-wire conditions.

Q12 Sketch a simple labelled diagram of a transformer-type transmission bridge. (*5 min*)

A12



Q13 Which of the following statements are descriptive of a transformer-type transmission bridge?

(*a*) *It acts as a high-pass filter and therefore has a non-uniform frequency response.*
(*b*) *It uses electromagnetic speech coupling.*
(*c*) *It requires high-impedance relays.*
(*d*) *It tends to eliminate longitudinal voltage surges.*
(*e*) *It is found in the final selector in non-director Strowger exchanges.*
(*f*) *It is found in TXE2 supervisory relay-sets.*
(*g*) *It is found in STD register access relay-sets.* (*5 min*)

A13 (*b*), (*d*), (*f*) and (*g*).

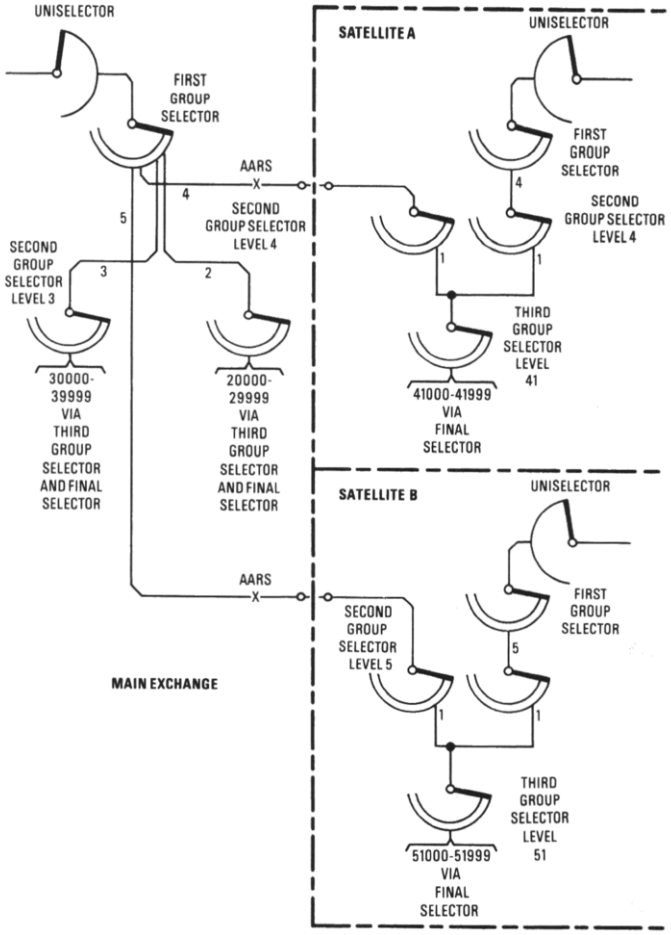
Q14 A Strowger multi-exchange linked-numbering-scheme area contains a main exchange and two group selector satellites. The ultimate capacities of each exchange are as follows:

Main exchange: 20 000 lines
Satellite A: 7 000 lines
Satellite B: 5 000 lines

Devise a suitable numbering scheme and draw a trunking diagram to show access to all local subscribers from the main exchange. (*15 min*)

A14 Numbering scheme:

Main exchange	20000–39999
Satellite A	41000–47999
Satellite B	51000–55999



Q15 On a Strowger exchange STD call, the equipment that stores dialled digits is:

(*a*) *the register access relay-set,*
(*b*) *the register,*
(*c*) *the translator, or*
(*d*) *the router control.* (*1 min*)

A15 (*b*) the register.

Q16 Define the term 'linked numbering scheme'. (*3 min*)

A16 A linked numbering scheme is one which is shared between several exchanges in a particular area. The same number is dialled for a particular subscriber irrespective of which exchange in the area it is dialled from; that is, no inter-exchange routeing digits need to be dialled.

Q17 Linked numbering schemes are used only in non-director areas. TRUE/FALSE. (*1 min*)

A17 False. [*Tutorial note:* All director areas, in fact, use linked numbering schemes by design.]

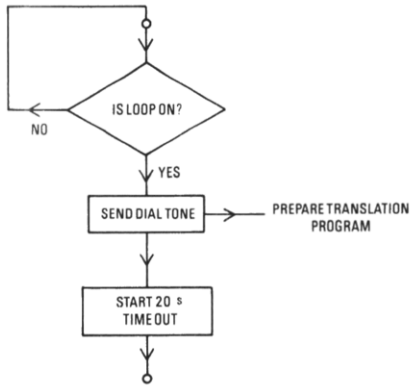
Q18 State three advantages of the director system as opposed to non-director systems in large urban areas. (*5 min*)

A18 Any three from the following:

(*a*) Uniform linked numbering scheme for the whole area.
(*b*) More efficient use of selectors, since translation allows very busy routes to be concentrated on one code selector stage, while less busy routes can be routed via several stages.
(*c*) Up to six translation digits allow calls to be routed in the most economical way.
(*d*) Routeings can be changed without affecting the published numbers.
(*e*) The control pulses generated by the exchange equipment can be more closely controlled and maintained than those produced by subscribers' dials.

Q19 For an SPC director exchange, draw a simple node transition diagram for the first scan of the processor on the setting up of an exchange call. (*5 min*)

A19



Q20 In a director exchange, the equipment replaced by SPC is:

(*a*) *the first code selector,*
(*b*) *the A-digit selector,*
(*c*) *the numerical selectors,*
(*d*) *the directors,*
(*e*) *the register access relay-sets,*
(*f*) *the local registers.*
(*g*) *the coin-and-fee check relay-sets.*

Choose three options. (*3 min*)

A20 (*b*), (*d*) and (*f*).

Q21 Which of the following was developed as a universal manual-board cord circuit:

(*a*) *bridge control,*
(*b*) *matrix,*
(*c*) *sleeve control, or*
(*d*) *cordless?* (*1 min*)

A21 (*c*) sleeve control.

Q22 With reference to a TXK1 crossbar exchange:

(*a*) *Name the five components that form the router.*
(*b*) *If the calling rate in a line distributor is high, what can be done to increase its traffic carrying capacity without affecting the number of DSA outlets?*
(*c*) *Explain the function of the start-shift circuit.*
(*d*) *For a 6000-line exchange, how many distributors are required?* (*10 min*)

A22 (*a*) (*i*) Transmission relay groups,
(*ii*) registers,
(*iii*) register allotter,
(*iv*) router switches A and B, and
(*v*) router control.

(*b*) In order to increase the traffic carrying capacity, the number of DSAs can be increased up to a maximum of 16 by fitting auxiliary DSAs in parallel with the regular DSAs. This effectively makes the DSA into a 20-inlet 25-outlet switch, giving access to an additional 5 originating and 5 terminating trunks.

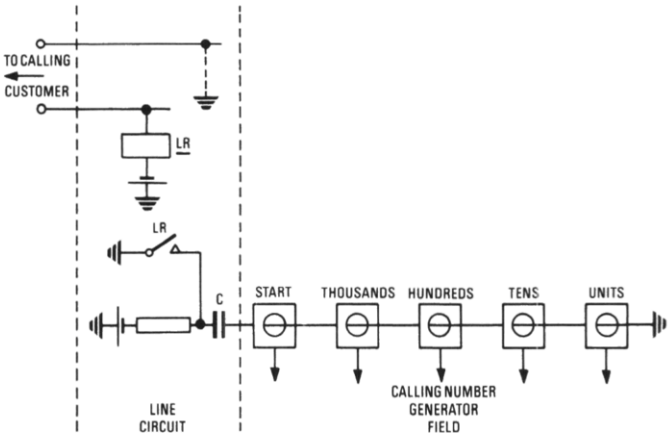
(*c*) The start-shift circuit ensures that only one call can be processed at any one time, regardless of the number of simultaneous calls in progress. Thus, only one set of marks can be applied at any time. It also ensures even spread of traffic over exchange equipment.
(*d*) Since each distributor serves 500 lines, then 12 distributors would be required for a 6000-line exchange.

Q23 For a TXE2 local electronic exchange:

(*a*) *Name four types of storage devices used.*
(*b*) *Explain with the aid of a simple block diagram how a calling line is identified.*
(*c*) *Explain why both directory numbers and equipment numbers are used.* (*10 min*)

A23 (*a*) (*i*) Reed relays,
(*ii*) silicon-controlled rectifiers,
(*iii*) bistable circuits, and
(*iv*) ferrite cores.

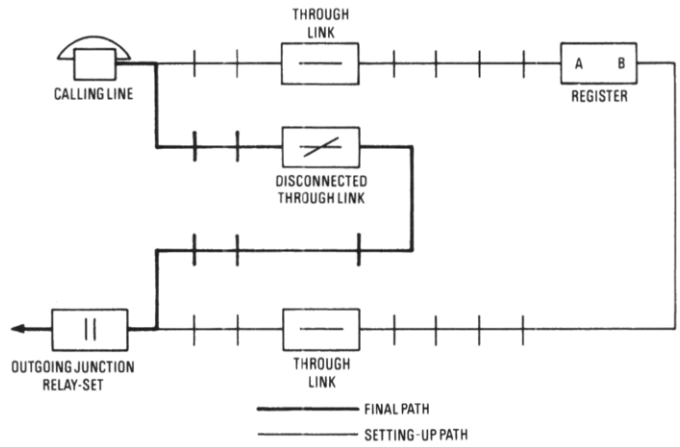
(*b*) An originating call causes the subscriber's line relay (LR) to operate, which, in turn, causes a capacitor to discharge through a jumper which passes through a unique combination of pulse transformers causing an output from each transformer secondary winding. Thus, each subscriber generates a unique code which is subsequently stored in the register and enables the line to be identified.



(*c*) In a TXE2 exchange, directory numbers have no association with the physical location of the caller's line circuit equipment. This provides considerable flexibility in allocating lines but it requires the conversion of directory numbers as generated by the calling-number generator into equivalent equipment numbers in order to locate the calling subscriber's line circuit.

Q24 Sketch a serial trunking sequence diagram for an outgoing junction call from a TXE4 exchange. (*5 min*)

A24



Q25 Explain the function of the scanner in a TXE4 exchange. (*3 min*)

A25 The scanner inspects each exchange termination at regular intervals in order to assess the state of the line.

MICROCOMPUTER SYSTEMS

Preface

GENERAL

This text has been written to provide an introduction to the world of the microcomputer for technicians in the telecommunications industry. An elementary knowledge of electrical and electronic circuitry, including some transistor theory and basic logic circuits has been assumed, but a comprehensive glossary is included which should be referred to by a reader who comes across an unfamiliar term. Although much of the text is general to all microprocessors, the Intel 8085 microprocessor is described when specific reference to one device is appropriate.

The text is written in six sections, which allows the reader to select those aspects of microcomputer technology in which his interest lies and pass over others. The contents of these sections are summarised as follows:

INTRODUCTION

The first section introduces the reader to the basic concept of a microcomputer.

NUMBERING SYSTEMS

This section reviews the numbering systems that are used with computer and microcomputer systems for those readers not familiar with this subject.

MICROPROCESSOR PROGRAMMING

This section deals with the way that instructions for the microcomputer are written (software). A glimpse is given into program writing, using a very simple example.

SYSTEM HARDWARE

This section deals with the physical components and support circuitry necessary to construct a complete system.

INSTRUCTION SET

An instruction set is a list of primitive instructions that a microprocessor accepts. This section lists the instruction set for the Intel 8085 microprocessor and is included to show the full range of instructions available for a typical microprocessor. This section is not intended for intensive study, but is for reference purposes.

GLOSSARY

This section includes definitions of terms used in this text.

This paper is a revised version of *Microcomputer Systems*, British Telecom Educational Pamphlet, Micro-electronics 1/1, Issue 1.1, January 1982.

Supplement to *British Telecommunications Engineering*, Vol 3. Part 3, October 1984.

Contents

Part 1

INTRODUCTION

Review

So much has been said and written about the capabilities of computers and microcomputers that it is easy to attribute intelligence to these machines. Arguably, a computer is incapable of intelligence, but merely obeys the instructions given to it. The most compelling attribute of a microcomputer is that, by the use of computer technology, one pack of components (set of hardware) can be instructed (programmed) to perform many different functions. The same microcomputer can serve at the heart of a digital voltmeter, a cash register, or a television game. This flexibility has brought microprocessor technology into the mass market, with all the resulting cost saving that this brings.

The first generation of electronic computers used thousands of thermionic valves. COLOSSUS, designed and constructed by the Post Office Research Branch at Bletchley Park in 1943, was one of the world's first and contained 1500 valves; such machines were extremely large and unreliable. In the next generation, the valves were replaced by transistors, which made them much more reliable, and reduced their size and cost. These solid-state machines raised the computer from being a laboratory curiosity to a useful practical device.

The 1960s saw the start of the integrated-circuit (IC) era. Third generation computers were built by using small-scale integration (SSI) devices. These devices had gates, bistable circuits, and similar circuits built into a single silicon chip. As semiconductor technology developed, medium-scale integration (MSI) ICs that contained complete counters, decoders, registers or adders were manufactured. As the miniaturisation trend continued, large-scale integration (LSI) devices that contained thousands of circuit elements on a single chip were introduced. The Post Office Research Laboratories at Dollis Hill designed a microprocessor-like device in 1969, but 1971 saw the introduction of the first commercially available microprocessor. This contained the major computation and control sections of a computer, called the *central processing unit (CPU)*, on a single IC chip.

Semiconductor memories were also developed and these LSI devices enabled thousands of bits of digital information to be stored on a single IC. LSI microprocessors and memory devices made possible the drastic reduction in size and cost of small computers, and allowed them to be built into many and varied products; at the same time, reliability and power consumption were improved.

Microprocessor-based designs, built with one or two ICs, can often replace a vast amount of circuitry built with discrete components. The miniaturisation of components integrated with all their interconnections within one silicon chip results in a smaller and more reliable product. Size reduction and increased reliability are also possible by using custom-designed ICs instead of microprocessors. However, the design of a custom-built IC can be extremely expensive and complex, and can be justified only where a high volume of production is involved. The development cost can then be spread over a large number of units. The microprocessor allows standard ICs to be used in many cases where LSI techniques would not normally be justified. Only the program that is stored in a memory needs to be custom built, and the production of a standard memory, with a specific program stored in it, is a relatively inexpensive process. However, program development costs can be considerable and so may cost in only where high-volume production allows them to be shared between a large number of final production items.

In addition to the great flexibility of microprocessor-based systems, their versitility makes possible many sophisticated features that were impracticable in the past. For example, cars can be fitted with microprocessors to optimise engine performance and fuel consumption under all conditions, and control the anti-skid braking system. Items passed in front of a scanner at a supermarket check-out terminal can be identified from a bar code; then, the item can be priced, the price printed on the customer's bill, and the inventory of the store updated automatically. It is even possible for the customer's bank account number to be entered and the money to pay for the bill automatically transferred from his bank account to the supermarket's account. Furthermore, because control is with the program (software), changes like price increases or changes in tax levels, are easy to make. The design of many products has indeed been revolutionised by the microprocessor. For British Telecom (BT), the microprocessor has already found hundreds of applications in both the engineering field as a controller and in the office environment as a computer.

The Basic Microprocessor System

In common with a main-frame computer, a microprocessor system, or microcomputer, comprises four basic parts or blocks; these four blocks are shown in Fig. 1.

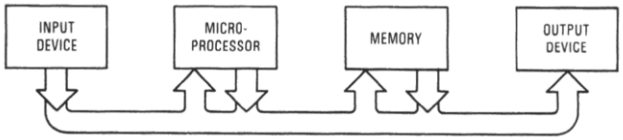


FIG. 1

The input device can take many forms; if a store cash register is taken as an example, the input device can be a keyboard. The microprocessor contains all the circuitry to enable the list of instructions (program) to be recognised and executed. The memory stores the program and can store other information (data).

The output device can also take many forms, and, for the store cash register example, an alphanumeric display or ticket printer would be appropriate.

The input and output devices of the system are known as *peripherals*, while the microprocessor and the memory form the microcomputer. The peripherals are connected to input and output ports within the microcomputer. These serve as the system interface. Within the microcomputer, information is passed along three information paths called *buses*. A bus consists of several conducting paths along which signals can be sent, in parallel, to the devices within the system.

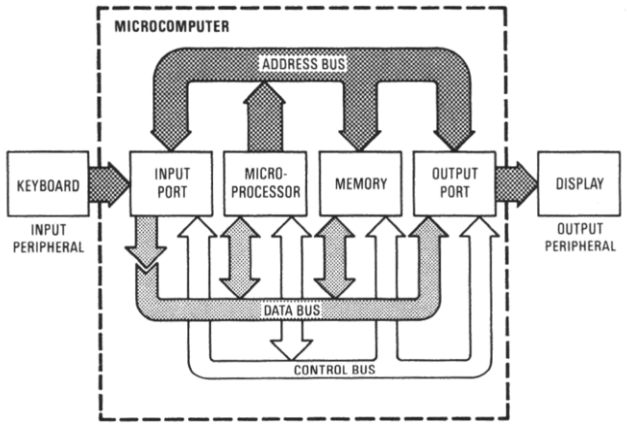


FIG. 2

Fig. 2 is a block diagram of a typical microcomputer, with a keyboard as the input peripheral and a visual display unit as the output peripheral. When a key on the keyboard is depressed, a signal is sent via an input port to the microprocessor along the control bus. This signal informs the microprocessor that data is ready for transfer. The microprocessor returns a control signal to the input port, which enables the data there to be transferred to the microprocessor along the data bus. Here, it can be manipulated as required. It might then be stored in a memory location. The microprocessor uses the address bus to select specific memory locations or input or output ports.

When a particular location or address has been selected, information, or data, is transferred via the data bus. Data can travel from the microprocessor to a memory location or output port, or from an input port or memory location to the microprocessor. Data does not usually go directly from one port to another or from the memory to a port.

When the output information is ready, the data is placed on the data bus and the output device enabled by control signals from the microprocessor.

Programs

Before a task can be performed by the system, explicit instructions are required. For example, instructions to display information about key depressions might be:

1 Read data from the keyboard.

2 Write data to the display.

3 Repeat (that is, go to step 1).

The list of instructions must then be translated into a language or code that the microprocessor can understand. The translated code is then stored in the memory of the system. The microprocessor then reads the first coded instructions from the memory, decodes the meaning of the instruction and performs the indicated operation. The instruction from the next memory location is then read and the corresponding operation is performed. The process is repeated, one memory location after another.

Certain instructions cause the microprocessor to jump out of sequence to another memory location. The new location could be to a previously executed instruction, and thus a loop which is executed repeatedly is created. Operations which must be repeated many times can thus be performed by a relatively short program.

The only code that the microprocessor can understand is in the form of binary information. A single digit of binary information (1 or 0) is called a *bit* (a contraction of *bi*nary digi*t*). One digital signal (HIGH or LOW, 5 V or 0 V) carries one bit of information. Microprocessors handle data, not as individual bits, but as groups of bits. The most common microprocessors in use at present have data buses which are either 8 or 16 bits wide; that is, one or two bytes wide. For simplicity, only 8 bit microprocessors are considered here. Note that the term *byte* as used in this text always implies eight bits. Similarly, the term *word* always means 16 bits (or two bytes). This usage, although very common, is not, unfortunately, universal.

A typical 8 bit microprocessor is the Intel 8085. On the data bus of the 8085, eight simultaneous signals (one byte) are conveyed within the microcomputer. With one byte, it is possible to individually address up to $2^8 = 256$ separate memory locations. Most microprocessor applications call for a much greater memory capacity than this, and so the address bus of the 8085 can carry 16 bits (2 bytes) of information, allowing $2^{16} = 65\,536$ separate locations to be addressed. Each memory location can hold one byte; therefore, if each address is used for a memory location, the memory could consist of $65\,536 \times 8 = 524\,288$ bits.

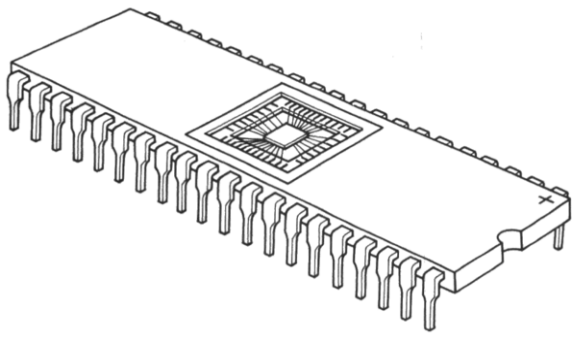
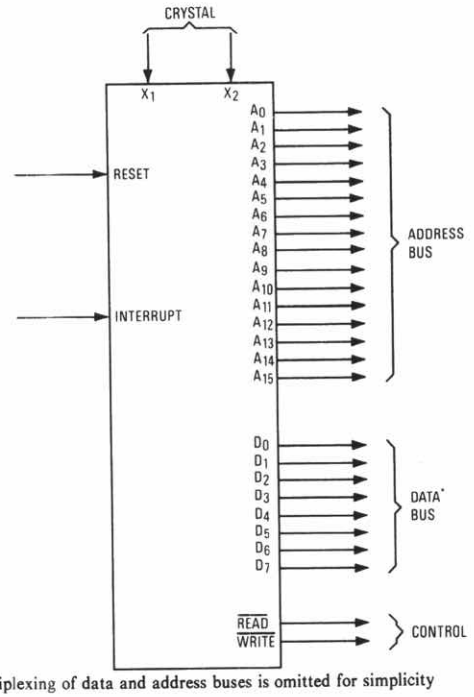


FIG. 3

Fig. 3 shows a section through an 8085 microprocessor package. The silicon chip and the wires bonding it to the external connections can be seen. The package has 40 pins which are connected via these thin wires to connection pads on the chip.



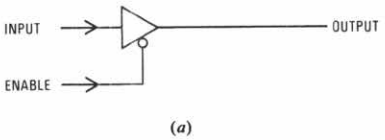
* The multiplexing of data and address buses is omitted for simplicity

FIG. 4

Fig. 4 shows the basic signals that are connected via the pins. There are 16 address outputs, which drive the address bus, and eight data pins, which connect to the data bus. The data pins are bidirectional so that data may go in or out of the microprocessor. *Read* and *write* signals co-ordinate the movement of data on the data bus. The RESET input is used to initiate the internal circuitry when the power is switched on. The INTERRUPT input allows the microprocessor to be diverted from its current program to another task which must be performed immediately. These and other signals are described later in the section on system hardware. The top two connections are for an external crystal, which is used to control the frequency of an oscillator in the microprocessor. The output of this oscillator is the system clock. The clock synchronises all the functions of the system and determines the basic rate at which instructions are executed.

Tri-State Drivers

Data can be put onto the data bus by the input ports, the microprocessor, or any of the memory locations. The microprocessor selects one device to place data on the bus and disconnects the others. So that the outputs of disconnected devices do not interfere with data on the bus when a data transfer is taking place, the connectors or drivers of these devices must have three states, LOGIC LOW (0 V), LOGIC HIGH (5 V) and high impedance (floating or no connection).



(*a*)

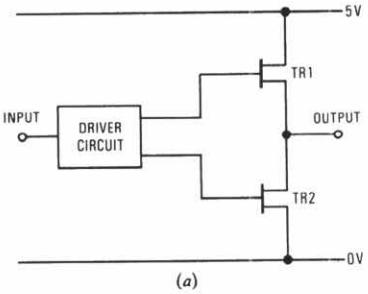
ENABLE	INPUT	OUTPUT
0	0	0
0	1	1
1	0	FLOATING
1	1	FLOATING

0 = LOW 1 = HIGH

(*b*)

FIG. 5

Fig. 5(*a*) shows the symbol and Fig. 5(*b*) the truth table of a tri-state driver (sometimes known as a *three-state buffer*). It has an additional ENABLE input as well as the normal input and output. When the signal on the ENABLE input is LOW, the device acts as a normal buffer amplifier. However, when the signal on the ENABLE goes HIGH, the output of the device is essentially disconnected.



(*a*)

TR1	TR2	OUTPUT
OFF	ON	0V
ON	OFF	5V
OFF	OFF	TRI-STATE

(*b*)

FIG. 6

A schematic diagram of a typical tri-state driver is shown in Fig. 6(*a*); transistors TR1 and TR2 are output transistors. The three states are achieved as shown in Fig. 6(*b*).

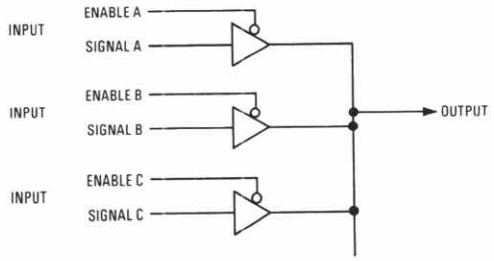


FIG. 7

Fig. 7 shows three signals connected to a common line. Only one driver is enabled at any one time to allow its associated signal to drive the output. If more than one driver were to be enabled, each signal would try to drive the output; the logic result would be unpredictable, and the drivers might be destroyed.

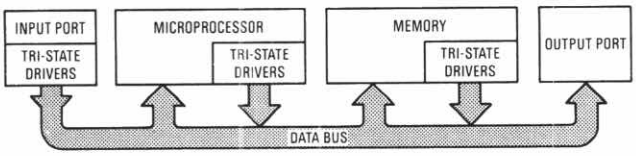


FIG. 8

Fig. 8 shows how tri-state drivers are used in microcomputer systems. The outputs of devices that put data on the data bus are buffered by tri-state drivers. The *enable* signals are generated by the microprocessor and conveyed via the control bus. Many ICs have internal tri-state drivers. An input pin, called *CHIP SELECT* or *CHIP ENABLE*, is provided and this controls the output drivers.

Memories

Microprocessor systems used for controlling applications usually store data and programs in IC memories. IC memories with a capacity of up to a quarter of a million bits on one chip are currently available. These ICs can store over 32 000 alphanumeric characters, or about 12 closely printed pages of text.

A simple form of memory device is a bistable circuit, which stores one bit of information. By using MSI technology, registers were built containing up to eight bistable circuits on a single chip, each with its own DATA-IN and DATA-OUT pins, but with a common CLOCK line. LSI technology enabled thousands of bistable circuits to be built on a single chip. However, this presented a problem of access to each bistable circuit: it is not practicable to construct an IC package with thousands of access pins. The use of address inputs to select the desired memory location (bistable circuit) solved the problem. A built-in decoder on the memory chip decodes the address and connects the selected memory location to the data pins.

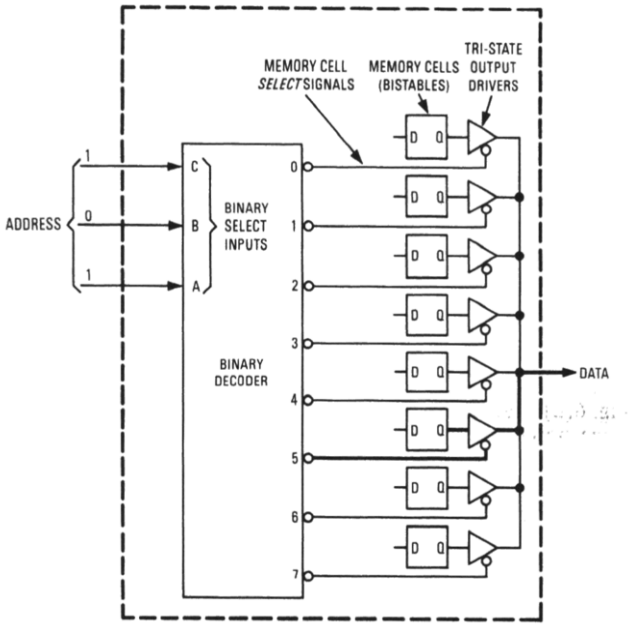


FIG. 9

The addressing concept is shown in Fig. 9. The binary decoder converts the binary address inputs into eight separate outputs, one for each of the possible combinations of the three address lines. These *select* signals control the tri-state drivers at the output of each bistable memory cell. The data from the addressed cell is put on to the single data output line.

The number of addressable locations depends on the number of address lines; for example, two locations can be addressed by using one address line; that is, address 0 and address 1. One of four locations can be selected by using two address lines; that is, 00, 01, 10, and 11. The general rule is:

$$\text{number of locations} = 2^n,$$

where n is the number of address lines.

Each memory location can contain a group of bits rather than just one. The number of bits contained in each location of an IC depends on the number of data pins. If an IC has eight data pins, each memory location of the IC can store eight bits of data. Note that, although the memory can contain thousands of locations, only one location can be accessed at any one time.

Memory ICs used within microprocessor systems fall into two main categories: read-only memory (ROM) and random-access memory (RAM). ROM is a memory that can only be read. The data is programmed into it during manufacture, or by a special programming procedure prior to its installation in the circuit. A program recorded into a ROM is often called *firmware*. Although 'random access' strictly means that the time to access any memory location is the same for any part of the memory, 'RAM' is widely used to describe IC read/write memory; that is, memory that data can not only be read from, but also written into, by the microprocessor.

Fig. 10 shows a photomicrograph of a BT designed and manufactured chip. A regular array of memory cells occupies the bottom two thirds of the picture.

Semiconductor RAMs are volatile. This means that, if their power supply is turned off, the data contained within the memory is lost. When power is restored, they contain unknown data, or rubbish. Permanent programs and data are therefore stored on ROMs, which do not suffer from this problem. RAMs must be used for temporary program and data storage as the contents of a ROM cannot be modified.

To summarise, the devices commonly called *ROMs* and *RAMs* are both 'random access' memory devices. ROMs retain their data even when the power is turned off, but cannot be written to by the processor. RAMs lose their data when the power is turned off, but can be written to by the microprocessor.

Developments in memory devices are eroding these differences so as to produce hybrid devices having the advantages of both ROMs and RAMs. Advances in technology also regularly increase the maximum data capacity of new memory devices.

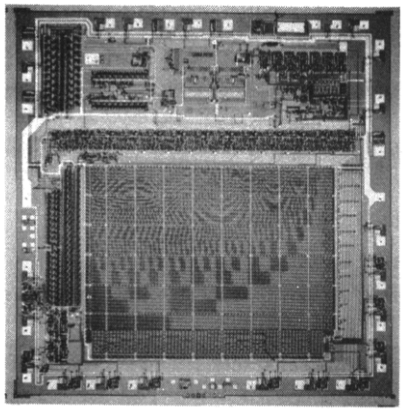


FIG. 10

Fig. 11 shows the address and data pin nomenclature of a ROM containing 2048 bytes (16 384 bits). When large numbers that are powers of two are used, K is often used to denote 1024 or 2^{10}. Thus, the memory shown in Fig. 11 can be described as a memory of 2K byte or 16K bit. Since each location contains eight bits, it is called a *2K × 8 ROM*. Tri-state output drivers

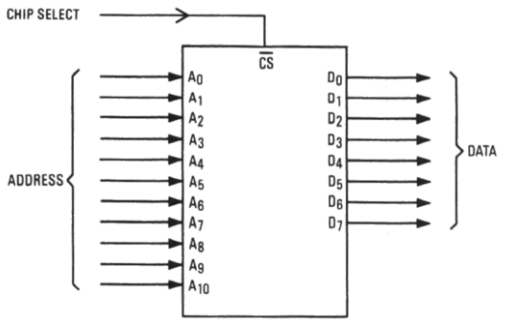


FIG. 11

are built onto the chip, and so many of these memory devices can be connected to the data bus; the required IC is then selected by a *chip select* signal. It is usual to find the CHIP SELECT input referred to as $\overline{CS}$†. This means that, when the $\overline{CS}$ input is LOW, the ROM's output drivers are enabled, and, when the $\overline{CS}$ input is HIGH, the data outputs are in the high-impedance state.

Fig. 12 depicts a 1K × 8 RAM. It contains 1024 locations of eight bits each. Data can go into or out of the memory, so the data lines are bidirectional. An additional READ/$\overline{\text{WRITE}}$ control line is provided that determines the direction of data transfer.

† $\overline{CS}$ is referred to as 'CS bar' or 'not CS'; the bar denotes negative logic.

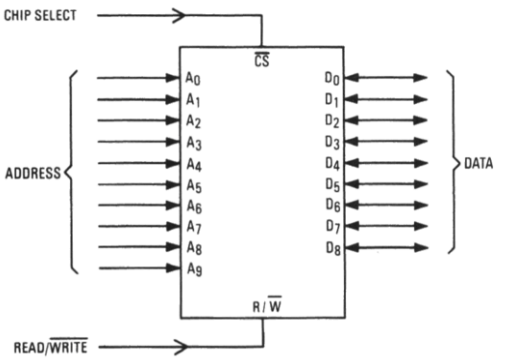


FIG. 12

A WRITE function is usually indicated when the line goes LOW. The line is often called $\overline{RD/WR}$ (or $\overline{R/W}$). The notation indicates that, if a HIGH signal is on the line, the READ function is selected, and, if the line goes LOW, a WRITE function is chosen. The IC must be addressed and the RD/$\overline{WR}$ input set before the CHIP SELECT line is pulsed. No transfer of data takes place until the *chip select* signal is HIGH.

NUMBERING SYSTEMS

Decimal and Binary

The numbering system that most people are accustomed to in their daily lives is the decimal system. This system has a radix or base of 10, which means that 10 different numbers (0–9) are represented by single characters. The possession of 10 digits on our hands probably had some bearing on the choice of 10 as a base.

A binary, or base 2, numbering system is much more suitable for use in computers. In this system, a single character can represent two different numbers, 0 and 1. A digital computer can therefore use an electrical signal to represent the digit. A 0 can be represented by a LOW signal state, while a HIGH signal is interpreted as a 1. Notice that it is not necessary to know the actual voltage level of the signal. Signal HIGH could be +5 V, with LOW as earth; or signal HIGH could be earth, with LOW as −5 V. The actual voltage is of interest only to the system hardware designer.

The position of a digit determines its weight or base power. In the decimal system, the digit positions, starting from a decimal point and moving to the left, have weights of $10^0 = 1$, $10^1 = 10$, $10^2 = 100$, $10^3 = 1000$, and so on. In the binary system, the weights are $2^0 = 1$, $2^1 = 2$, $2^2 = 4$, $2^3 = 8$, and so on. Table 1 compares the decimal and binary weightings.

TABLE 1

Decimal	Binary
$10^0 = 1$	$2^0 = 1$
$10^1 = 10$	$2^1 = 2$
$10^2 = 100$	$2^2 = 4$
$10^3 = 1000$	$2^3 = 8$
$10^4 = 10\,000$	$2^4 = 16$
$10^5 = 100\,000$	$2^5 = 32$

To convert from binary to decimal forms, the decimal values of the columns are simply added together. For example:

$$11001 = (1 \times 2^0) + (0 \times 2^1) + (0 \times 2^2) + (1 \times 2^3) + (1 \times 2^4),$$

$$= 1 + 0 + 0 + 8 + 16 = 25.$$

Where confusion could arise, the base value can be added as a subscript to the number; that is,

$$11001_2 = 25_{10}.$$

Fig. 13 shows a technique for converting numbers from decimal to binary form. The decimal number is divided by 2. The remainder (1 in the example) becomes the least significant bit of the result. The result of the division (6 in the example) is then divided by 2 again, the remainder becoming the second bit of the result. This process is continued until the result of the division is zero.

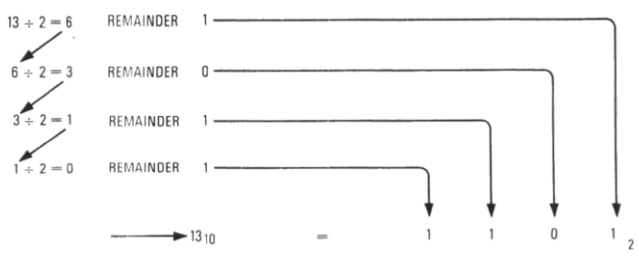


FIG. 13

Octal Numbering System

Binary numbers, in general, contain many more digits than their decimal equivalent. This makes them more difficult to handle. For example, when the number 10110001 is being copied, it is easy to make a mistake and write 10111001. To reduce the chance of making mistakes, a more compact representation of binary numbers is needed. Decimal numbers could be used, but conversion between decimal and binary numbers is awkward. Fig. 14 shows a representation called *octal*, which uses a radix or base of 8.

FIG. 14

The binary number (011110010) is divided into groups of three bits, starting on the right. Each group of three bits is then replaced by its octal equivalent. Thus 011 110 010 becomes 362 octal. The binary number 110 100 can therefore be represented by the octal number 64. Note that, although octal numbers look like decimal numbers, their value is different. The decimal equivalent of 110 100 is

$$2^2 + 2^4 + 2^5 = 52.$$

It is much easier to convert between binary and octal numbers than between binary and decimal. Although popular at one time, the octal system has been largely replaced by the hexadecimal system.

Hexadecimal Numbering System

Another convenient representation for binary numbers is a system with a radix or base of 16. In the hexadecimal system, each group of four binary digits is replaced by a single character. Thus, 01010011 becomes 53. Since four bits can have decimal values from 0 to 15, a way is needed to represent the decimal values 10 to 15 with a single character. The letters A to F are used for this purpose. Hexadecimal numbers are often denoted by the word 'hex' or by the subscript H at the end of the number. Table 2 shows the binary and hexadecimal values of the decimal numbers 0 to 15.

TABLE 2

Binary	Hexadecimal
0000	0
0001	1
0010	2
0011	3
0100	4
0101	5
0110	6
0111	7
1000	8
1001	9
1010	A
1011	B
1100	C
1101	D
1110	E
1111	F

Once the use of A to represent 10, B for 11, etc., is mastered, conversion from binary to hexadecimal and from hexadecimal to binary forms is easy.

For use with microprocessors, the hexadecimal system is the most widely used system for representing binary numbers. An 8 bit binary number can be represented with two hexadecimal

characters, while three octal characters are needed to do the same thing. The hexadecimal representation is therefore more compact and results in less potential errors when keying in.

Table 3 compares binary, decimal, octal and hexadecimal values.

TABLE 3

Binary	Decimal	Octal	Hexadecimal
00000	0	0	0
00001	1	1	1
00010	2	2	2
00011	3	3	3
00100	4	4	4
00101	5	5	5
00110	6	6	6
00111	7	7	7
01000	8	10	8
01001	9	11	9
01010	10	12	A
01011	11	13	B
01100	12	14	C
01101	13	15	D
01110	14	16	E
01111	15	17	F
10000	16	20	10
10001	17	21	11
10010	18	22	12
10011	19	23	13
10100	20	24	14
10101	21	25	15
10110	22	26	16
10111	23	27	17
11000	24	30	18
11001	25	31	19
11010	26	32	1A
11011	27	33	1B
11100	28	34	1C
11101	29	35	1D
11110	30	36	1E
11111	31	37	1F

Bit Position Convention

When binary numbers are referred to, it is often necessary to refer to a particular bit. The right-hand side bit is called the *least-significant bit (LSB)*, and the left-hand bit is called the *most-significant bit (MSB)*. When a group of bits at one end of a word are referred to, the left-hand bits are called the *high-order* (or *most-significant*) *bits*, and the right-hand bits are called the *low-order* (or *least-significant*) *bits*.

Binary-Coded Decimal Representation

Most microprocessor systems have decimal input and output devices, such as keyboards and displays. The decimal numbers obtained from, or supplied to, these devices must be represented in a binary form for manipulation within the processor. For example, if the decimal number 29 is read from a keyboard, it can be converted to its binary equivalent, 00011101 ($1D_H$). If, then, the number is required to be displayed on a decimal display, it must be converted back to the two decimal digits 2 and 9.

An alternative method is to take each of the decimal digits, 2 and 9, and convert them independently into two 4 bit binary numbers. These two 4 bit numbers are then packed into one byte. Thus, 29 would be coded as 0010 1001. The binary values 1010 to 1111 (A_H to F_H) are never used in this representation, which is known as *binary-coded decimal (BCD)*.

A disadvantage of BCD is its inefficient use of storage space. One 8 bit byte can store a number up to a value of only 99 by using BCD, whereas a value of 255 can be stored by using pure binary. This is because the hexadecimal values A to F are not used.

Binary Arithmetic

Numbers represented in binary form can be added in exactly the same way as decimal numbers if the following rules are obeyed:

$$0 + 0 = 0$$
$$0 + 1 = 1$$
$$1 + 0 = 1$$
$$1 + 1 = 0 \text{ and 1 to carry}$$

For example,

$$\begin{array}{r} 10110011 \\ +01100111 \\ \hline 100011010 \end{array}$$

Subtraction, can be performed in the same conventional way, but it is usual for microprocessors to use the method of two's complement addition.

Negative Numbers

Consider Table 4.

The table is formed by decrementing (subtracting 1 from) the positive integer 7 in both the decimal and binary forms. Notice that, when zero is decremented, it becomes −1 or binary 1111 1111. This binary form is known as the *two's complement of 1*. Two's complement allows the representation of negative numbers. In the two's complement representation, the MSB

TABLE 4

Decimal	Binary
7	0000 0111
6	0000 0110
5	0000 0101
4	0000 0100
3	0000 0011
2	0000 0010
1	0000 0001
0	0000 0000
−1	1111 1111
−2	1111 1110
−3	1111 1101
−4	1111 1100
−5	1111 1011
−6	1111 1010
−7	1111 1001
−8	1111 1000

indicates the sign. If the MSB is 0, the number is positive; if the MSB is 1, the number is negative. This representation allows numbers of positive 127 to negative 128 to be defined by using an 8 bit word.

Note that the number 1111 1011 can also be interpreted as 251 decimal, if it were considered to be straight binary rather than two's complement. It is therefore necessary to know which of these two forms is appropriate and to treat the number accordingly.

Two's-Complement Arithmetic.

The two's complement of a number is easily found. The procedure is as follows:

1 Write the binary value (using eight bits since an 8 bit microprocessor is being considered); that is, for 5 write 0000 0101.

2 Complement the binary number (change the ones to zeros and the zeros to ones). This is called the *one's complement*; that is, 0000 0101 becomes 1111 1010.

3 Add 1 to form the two's complement; that is,

1111 1010 + 1 = 1111 1011.

This procedure is very easily and automatically carried out in a microprocessor system.

Subtraction is carried out by the addition of the two's complement.

For example,

$$0111\ 0100 - 0110\ 0111$$

is evaluated as

$$0111\ 0100 + 1001\ 1001$$

that is,

$$\begin{array}{r} 0111\ 0100 \\ +1001\ 1001 \\ \hline 1\ 0000\ 1101 = 13_{10} \end{array}$$

The '1' overflow is ignored.

Multiplication of two numbers can be achieved by successive addition of the multiplier (faster multiplication techniques are, however, normally used); division can be achieved by successive subtraction of the divisor, and this is, in fact, a series of additions of the two's complement of the divisor. Thus, all the arithmetic operations can be carried out by using only simple adding circuits.

Mathematical Algorithms

Even complex mathematical functions can be evaluated (or approximated very closely) by using simple addition and two's complement addition. Techniques for performing a given operation are called *algorithms*. For example, the equation:

$$\sin x = x - \frac{x^3}{3 \times 2} + \frac{x^5}{5 \times 4 \times 3 \times 2} - \frac{x^7}{7 \times 6 \times 5 \times 4 \times 3 \times 2 \times 1} + \frac{x^9}{9 \times 8 \times 7 \times 6 \times 5 \times 4 \times 3 \times 2} - \cdots\cdots\cdots$$

is an infinite series which gives an exact value for the sine of an angle if it is evaluated for an infinite number of terms. Multiplication and division are used, but they can be performed by using the methods previously described. In practice, of course, only a finite number of terms can be calculated, and the result is an approximation, but very accurate if many terms are used.

The series above provides an algorithm for calculating the sine of an angle. For every mathematical function there is an algorithm that allows the function to be calculated by using only the elementary operations that a microprocessor can perform.

Large and Small Numbers

There are several different ways in which the range of numbers that can be represented by using 8 bit bytes can be extended. The method used depends upon how wide a range is required, and the degree of precision needed.

Double Precision

The simplest technique for extending the range is simply to increase the number of bits used to represent each number. This is often done by using pairs of 8 bit bytes to represent a single number.

This technique is represented in Fig. 15.

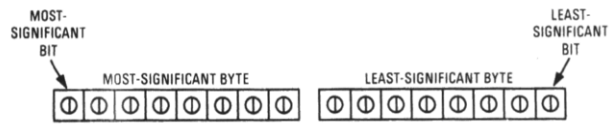


FIG. 15

The 8085 microprocessor contains a number of register pairs and, by using the register pair instructions, 16 bits can be operated on at a time. The use of two bytes for one number, known as *double precision* representation, extends the range of numbers that can be handled by an 8 bit processor to 0–65 535 or ±32 767.

Fixed Point

Double precision representation extends the range of magnitude, but numbers that have a fractional component need a different method of representation.

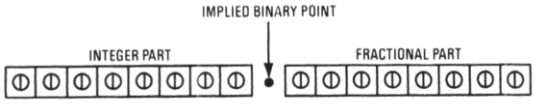


FIG. 16

Fig. 16 shows a representation called *fixed point*. Two bytes are used to store the number; the first byte, defined as being to the left of the decimal (or binary) point, contains the integer part, and the second byte, to the right of the binary point, contains the fractional part. The resolution is limited to $2^{-8} = 1/256$ (about 0·004) and the range to ±127.

Floating Point

Fixed point representation can be extended by using multiple bytes for each part of the number, but, unless a large amount of memory is dedicated to each number, it is still incapable of representing numbers such as 360 000 000 000 or 0·000 000 297. However, these numbers can easily be represented by using scientific notation, or mantissa and exponent. The mantissa is the magnitude of the number adjusted to between zero and one. The number 360 000 000 000 for example can be written as $0{\cdot}36 \times 10^{12}$ (0·36 is the mantissa and the exponent is 12). The number 0·000 000 297 can be written as $0{\cdot}297 \times 10^{-6}$ (0·297 is the mantissa and −6 is the exponent).

If two bytes are used to represent each number, as shown in Fig. 17, the range of values that can be represented, assuming that both mantissa and exponent are stored in two's complement form, is $\pm 10^{\pm 127}$. This is a very large range; 10^{127} is a very large number and 10^{-127} is very small.

FIG. 17

Alphanumeric Representation

Many microprocessor systems must operate not only on numbers, but also with letters. For example, a computer terminal must read the characters from the keyboard and send them to the computer. Letters must somehow be represented by binary numbers.

Fig. 18 shows the most popular code for representing alphanumerics. It is known as the *American standard code for information interchange (ASCII)*.

Every character is assigned a binary value. It was found that a maximum of 128 different characters are needed and, as this number can be represented by using a 7 bit binary number, only 7 bits are necessary to represent the ASCII characters. The most significant bit where an 8 bit code is being used is therefore zero*. The next three most-significant bits (bits 7, 6, and 5 in Fig. 18) select a particular column of characters from the table, and the least-significant four bits select the row. As with all

* Some modern printers and visual display units use this eighth bit to denote special character features; for example, italic or normal print, reverse video or normal video. However, this use is not standardised.

BITS 4321 765	000	001	010	011	100	101	110	111
0000	NUL	DLF	SP	0	@	P	`	p
0001	SOH	DC1	!	1	A	Q	a	q
0010	STX	DC2	"	2	B	R	b	r
0011	ETX	DC3	#	3	C	S	c	s
0100	EOT	DC4	S	4	D	T	d	t
0101	ENQ	NAK	%	5	E	U	e	u
0110	ACK	SYN	&	6	F	V	f	v
0111	BEL	ETB	'	7	G	W	g	w
1000	BS	CAN	(	8	H	X	h	x
1001	HT	EM	)	9	I	Y	i	y
1010	LF	SUB	*	:	J	Z	j	z
1011	VT	ESC	+	;	K	[	k	{
1100	FF	FS	,	<	L	\	l	¦
1101	CR	GS	–	=	M	]	m	}
1110	SO	RS	.	>	N	^	n	~
1111	SI	US	/	?	O	_	o	DEL

FIG. 18

representations, the context of the information is important. For example, 0101 0100 can be the binary representation of the number 84, the BCD representation of 54, or the ASCII character T. The codes in the shaded areas are control codes, which provide special functions. The code 0000 1010, for example, is used to cause a line feed on a printer or display.

The assignment of codes to characters is arbitary, and there are many other possibilities besides ASCII. ASCII is currently the most widely used code, but, in the past, a code called *BAUDOT* was very popular, and IBM machines use extended binary-coded decimal interchange code (EBCDIC).

Table Look-Up

A common programming problem is the conversion of one number representation or code to another. For example, consider the problem of displaying a hexadecimal digit on a 7-segment display. The segments that must be turned on to display the appropriate character must somehow be determined. A conversion from binary to 7-segment code is therefore required.

This conversion is done by using a technique called *table look-up*. The segment patterns for each character are stored as a list in memory called a *table*. The first entry contains the segment pattern for the character 0, the next for the character 1, and so on. To translate a binary code to the corresponding 7-segment code, the code is simply 'looked-up' in the table. For example, when the address for binary 1 is read, the readout is in 7-segment code form.

MICROPROCESSOR PROGRAMMING

Software Fundamentals

A microcomputer system consists of both hardware and software. It is the software (or program) which tells the system what to do. When the power to the system is switched on, the system usually starts a simple ROM-based program running automatically (for example, a boot-strap loader, a monitor or a system control program). Such programs perform initialising functions, perhaps make diagnostic checks on hardware and then permit a main program to be loaded into RAM from disc or tape. In the case of a computer system dedicated to one task, the main program (and any initialising routines) are normally present in ROM and not loaded separately.

When writing a computer program, the programmer must tell the computer what to do down to the most minute detail. The instructions are stored sequentially in the computer memory and, unless special instructions are included to change the sequence (JUMP, CALL, or BRANCH instructions), they are dealt with sequentially by the microprocessor.

The list of all possible binary instructions understood by the computer is called the *instruction set*. Instruction sets vary from one type of microprocessor to another, but they all have certain features in common. The operations are essentially simple in themselves and can be grouped as follows:

(*a*) data transfer operations;
(*b*) arithmetic operations (ADD, SUBTRACT, SHIFT, INCREMENT, DECREMENT);
(*c*) logical comparison operations (AND, OR, EXCLUSIVE-OR);
(*d*) program-sequence control (JUMP, CALL, BRANCH);
(*e*) input/output operations; and
(*f*) internal control operations.

There are 256 (2^8) different binary patterns that can be placed on the eight lines of an 8 bit data bus, and so 256 different instructions are, in principle, possible. The 8085 makes use of 246 of these patterns, one for each different instruction. The remaining 10 patterns have no meaning and are not used by the programmer.

The instruction set for the 8085 microprocessor is included in a later section.

Writing a Program

Before an attempt is made to write a program, the problem to be solved, or the logical function required, must be clearly set down; this task is sometimes called *systems analysis*.

The next stage might be to draw a diagram showing the operations required. It then becomes much easier to write the program. To illustrate the procedure, consider using a microprocessor as a simple AND gate.

The Requirements

An input port with an input channel for each input of the simulated AND gate is required.

The AND function can be performed by using instructions stored within the system memory.

Since an AND gate has only one output, only one bit of the output port is needed.

Fig. 19 shows a block diagram of the arrangement.

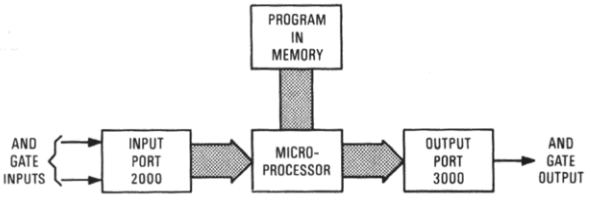


FIG. 19

Flow Charts

A flow chart is one graphical way of describing the operation of a program. It is composed of different types of blocks interconnected with lines. The three principal types of blocks used for flow charts are shown in Fig. 20. A rectangular block describes each action the program takes. A diamond-shaped block is used for each decision, such as testing the value of a variable. An oval-shaped block marks the beginning of the flow chart, with the name of the program placed inside it. An oval can also be used to mark the end of the flow chart.

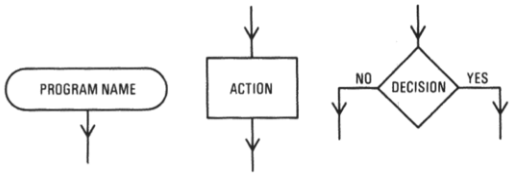


FIG. 20

Fig. 21 shows a flow chart for the AND gate. There is a block for each line of the program, except for the two GOTO instructions; these are represented simply by a line. The lines show the flow of the program from one block to another.

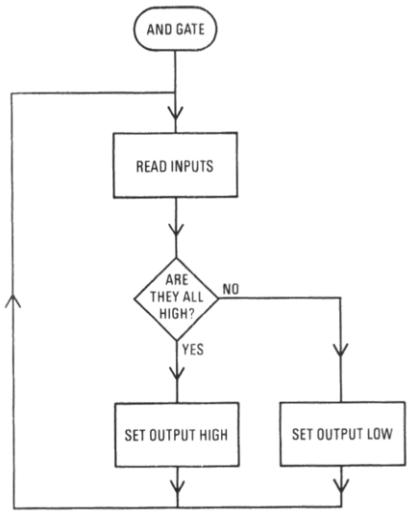


FIG. 21

First, the input port is read. Then the inputs are examined to see if they are all HIGH, since that is the function of an AND gate. If the inputs are all HIGH, the output is set HIGH; otherwise, it is set LOW. Once the procedure has been completed, the program jumps back to the beginning and repeats indefinitely, so that the output continuously follows changes in the inputs.

Other Graphical Methods

Professional programmers now prefer alternative graphical representations of programs to flow charts. The fall-back diagram and program description language (PDL) are two examples. Both permit better structured program design. PDL involves mostly words and might not be regarded as a graphical technique at all. This area is too involved to be discussed here, but the reader should be aware that good program design is not easy and only relatively recently have many of the preferred design tools been made easily available. The flow chart will probably be used in the future for only short routines written in low-level languages.

Programming Exercise

As an exercise, readers may like to construct a flow chart for programming a microcomputer to perform the logical OR function.

Solution

A solution to this problem is shown in Fig. 22. The input ports are read and then examined to see if all inputs are LOW; if so, the output is set LOW. If any input is HIGH, the output is set HIGH. The procedure is repeated indefinitely to follow changes in the inputs.

Programming Language

The flow chart must now be converted to a program; that is, a list of instructions for the microprocessor to execute. The microprocessor requires that the program should be in the form of a series of binary digits; that is, in machine code. But writing in this form is very difficult and tedious. If the list for the AND function example is written in plain human language, it might appear as follows:

1 Read the input port.

2 Go to step 5 if all inputs are HIGH; otherwise, continue.

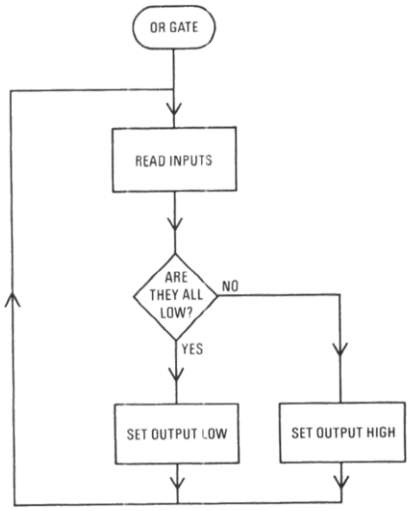


FIG. 22

3 Set output LOW.

4 Go to step 1.

5 Set output HIGH.

6 Go to step 1.

However, this list would not be understood by the computer.

To overcome the problem, high-level computer languages have been developed. These languages consist of a number of English-like statements that can, with practice, be used by the program writer, and then, with the aid of a computer program called a *compiler*, be translated into the required computer machine code. Different high-level languages are available for different computing tasks. FORTRAN, which emerged from IBM in 1957, became popular for scientific applications. For commercial data processing, COBOL became even more popular. Other popular languages include ALGOL and PL/1, while special-purpose languages include LISP for list processing, SNOBOL for string handling, and CORAL 66 for real-time applications. BT has used a variant of CORAL 66, known as *PO CORAL*, for use with System X; and PLM, a variant of PL/1. In the future, advanced languages such as CHILL (the CCITT *HI*gh *L*evel *L*anguage) and ADA (from the American Defense Department) will find much use. For teaching purposes, two common languages are available:

(*a*) *BASIC* (*B*eginners *A*ll-purpose *S*ymbolic *I*nstruction *C*ode) This language is widely used but is suitable only for simple programs because of its unwieldy structure.

(*b*) *PASCAL* This language is a descendant of ALGOL, CORAL and PLM and, while slightly harder to learn than BASIC, is much preferred because of the many advantages it offers. It also leads naturally towards CHILL and ADA in its structure.

Assembly Language

Assembly language is a low-level language; it is a system of mnemonics which represents, on a one-to-one basis, the instruction digits of a machine code. All instruction sets have their own sets of mnemonics, but all follow a basic pattern. Although it is much more difficult to write a program in assembly language than it is in a high-level language, there are certain advantages. Small programs, subroutines or programs where speed or efficiency is pertinent are often written in assembly language. Assembly language also allows certain operations which may not be possible in a high-level language.

Before the program for the AND gate can be written for running on a particular machine, several variables need definition. The address of the input port must be known. There are eight separate input channels to each input port. Any channel of the port in use that is not used for an input signal should be set to ONE.

The address of the input port could be a 16-digit binary number, but it is easier to use the 4-digit hexadecimal form. Likewise, the output port has eight channels; as the AND function is being used, the channels all contain the same information and so increase the effective 'fan out' of the gate. For this example, the input port is given an address of 2000_H, and the output port an address of 3000_H.

The first instruction is to read the information at the input port and load it into a register in the microprocessor known as the *A register* or *accumulator*.

This can be written in an assembly language as:

1 LDA 2000_H

The input signals are now in the accumulator, and the next problem is to see if all eight bits are ONE. There is no straightforward test, but if all eight bits are ONE and 1 is added, all eight bits go to ZERO (the 1 that is carried over sets a flag within the microprocessor). If any of the eight bits are ZERO, adding 1 would not cause all ZEROs to appear. When all the eight bits of the accumulator are ZERO after an arithmetic operation, a flag is set which can be tested.

Instruction 2 is therefore:

2 INR A (Add 1 to the contents of register A)

The next instruction tests the accumulator and causes the program to jump to the step specified if the *zero* flag is set. (The *zero* flag is a specific bit in a register called the *flag register* and is set to ONE when all the eight bits of the accumulator are set to ZERO.)

3 JZ Step 7

If the *zero* flag is not set, the program continues. The output port must now be set to ZERO. To do this, the accumulator is set to ZERO, and then the contents of the accumulator are transferred to the output port. A simple way to set the accumulator to ZERO is to subtract its contents from itself. Instruction 4 is therefore:

4 SUB A

Instruction 5 becomes:

5 STA 3000_H (Load output port with the contents of the accumulator; that is, ZERO)

Instruction 6 is:

6 JMP 1 (Return to the start)

If the *zero* flag had been set at instruction 3, the accumulator would have contained all ZEROs, but the output port needs to be set to ONE. The answer is to complement the accumulator before the output port is loaded. Instruction 7 is therefore:

7 CMA (Complement the accumulator; that is, set it to ONEs)

Instruction 8 is:

8 STA 3000_H (Load output port with ONEs)

Instruction 9 is:

9 JMP 1 (Return to the start)

The complete program, written in 8085 assembly language, is as shown in Table 5.

Refinements to this program are possible, but the program developed here works as it stands.

Although the program is now in assembly language, there is still one more step to go before it can be fed into the system; that is, translate the program into machine code. Machine code is a set of binary numbers. The assembly code is therefore translated into binary code either by using a conversion chart for the particular microprocessor being used, or a computer program called an *assembler*. The program is then loaded into RAM in the system memory, starting at say location 8000_H, for example. For convenience, the binary machine code is expressed in hexadecimal form.

Thus, LDA 2000_H becomes:

8000 3A
8001 00
8002 20

Step 1 starts at memory location 8000_H, which contains $3A_H$ (LDA).

Memory location 8001_H contains the least-significant byte of location 2000_H, and location 8002_H contains the most-significant byte.

Step 2 is stored in memory location 8003_H, which contains $3C_H$ (INR A). The complete program is now written as shown in Table 6.

TABLE 5

Label	Mnemonic
START	LDA 2000H
	INR A
	JZ YES
	SUB A
	STA 3000H
	JMP START
YES	CMA
	STA 3000H
	JMP START

TABLE 6

Label	Address	Machine Code	Mnemonic
START	8000	3A 00 20	LDA 2000H
	8003	3C	INR A
	8004	CA 0E 80	JZ YES
	8007	97	SUB A
	8008	32 00 30	STA 3000H
	800B	C3 00 80	JMP START
YES	800E	2F	CMA
	800F	32 00 30	STA 3000H
	8012	C3 00 80	JMP START

It can be seen that each mnemonic results in one or three bytes of machine code. Other instructions exist which result in two bytes, and certain other processors can have four or even more bytes to each instruction.

Review of Programming Steps

The steps involved in preparing a program are as follows:

Step 1 The problem to be solved must be clearly stated.

Step 2 A graphical description is made of the program.

Step 3 Either

(*a*) the graphical description is written in a high-level language such as PLM or PASCAL; or

(*b*) the graphical description is expanded into the elementary instructions of a low-level language, which would normally be assembly language.

Step 4 The high-level language is converted to machine code by a compiler program, or the assembly language is converted to machine code by an assembler program.

Step 5 The program, in binary form, can then be stored in the memory of the system. The memory varies from one type of system to another. Many microprocessor systems use a 16 bit address bus, and this allows the use of memory addresses from 0000_H to $FFFF_H$. Not all of these addresses are available to the programmer however. Part of the memory space (usually low-numbered addresses) are used for system operating programs stored in ROM. Some of the address space can be used for input and output ports, and there may be blocks of address space that are spare and not provided with memory chips. These addresses can be used for system expansion. The address of the RAM that is available to the programmer must be known, as well as the address of any input or output ports or peripherals that may be required.

The address of a particular location consists of 16 binary or four hexadecimal characters; therefore, as each address can hold only eight binary or two hexadecimal characters, two locations are needed to hold an address. It is necessary to store the lowest-significant byte of the address in the first location and the highest-significant byte in the next location in the case of the 8085 and many other 8 bit processors.

Programming Exercise

The reader is invited to use the OR gate flow chart complied earlier and write a program in assembly language for the 8085 microprocessor to perform the OR function. The input port address could be 2000_H and the output port address 3000_H. Although many of the instructions needed have been described earlier, the following additional instructions may need to be used:

(*a*) *JNZ* This instruction performs the opposite to JZ; it causes the program to jump if the *zero* flag is not ZERO.

(*b*) *CPI number* This instruction compares the accumulator with the *number* to test for a match.

(*c*) *MVI A, number* This instruction places any number from 0 to 255 into the accumulator.

(Full details of these instructions and all 8085 instructions are given in Part 2 of this text.)

Assume the program starts at 8000_H and that unused inputs are strapped to LOGIC ZERO.

Solution

A solution is as shown in Table 7.

TABLE 7

Label	Address	Machine Code	Mnemonic
START	8000	3A 00 20	LDA 2000H
	8003	FE 00	CPI 00H
	8005	C2 0E 80	JNZ NO
OUT	8008	32 00 30	STA 3000H
	800B	C3 00 80	JMP START
NO	800E	3E FF	MVI A, 0FFH
	8010	C3 08 80	JMP OUT

The reader should not be surprised if the program arrived at is different from the above solution. There are many valid variations that solve the problem. Notice the economy of the last instruction, which replaces two instructions that were used in the AND gate example. The penultimate instruction contains the number $0FF_H$. The leading zero is included as, for many assemblers, numeric quantities must start with a number not a letter; a zero is always inserted before any hexadecimal number which starts with A, B, C, D, E or F.

Internal Register Organisation

Fig. 23 shows the arrangement of the registers within the 8085 microprocessor. The A register, or accumulator, is used for all arithmetic or logical operations and is an 8 bit register.

The flag register also has eight bits, but only five of these bits are used. The S indicates the *sign* flag; Z, the *zero* flag; AC, the *auxiliary carry* flag; P, the *parity* flag; and C, the *carry* flag. The bits marked X are undefined.

The 8 bit registers B and C, and D and E are often used as register pairs, when 16 bits of information need to be stored.

Registers H and L can be used to hold a 16 bit address, the 'high' byte being stored in register H and the 'low' byte in register L. The address stored in the H and L registers is known as the *M (memory) address*.

The program counter holds the address of the next instruction to be executed.

The first address of a program is loaded into the counter to start the program. The counter is incremented every time an instruction is executed.

The stack pointer is a 16 bit register that is used mostly in conjunction with subroutines (auxiliary programs used by the main program).

The advantage of a subroutine (also called a *procedure*) is that, although many parts of the main program may use it, it occurs only once in memory. The problem that results is how to direct the program flow back to the correct part of the main program after completion of the subroutine. An area of memory, known as *stack memory*, provides a neat solution. The main

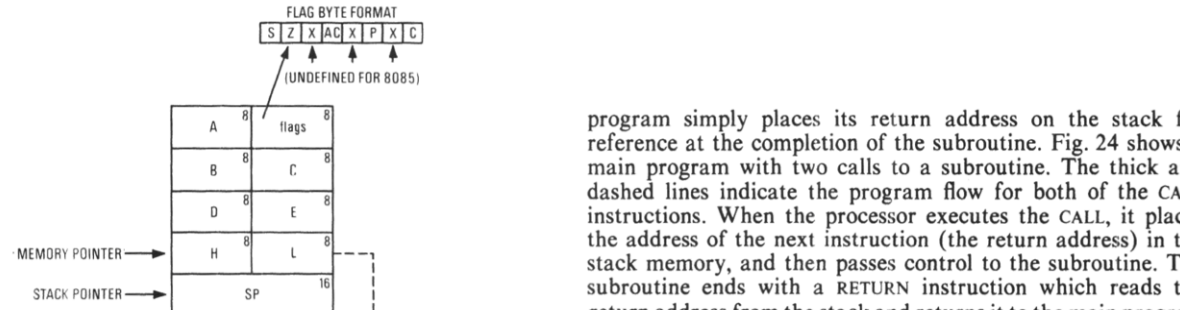


FIG. 23

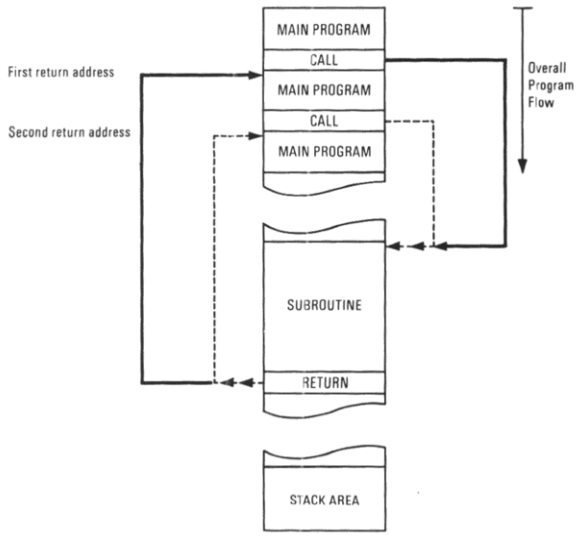


FIG. 24

program simply places its return address on the stack for reference at the completion of the subroutine. Fig. 24 shows a main program with two calls to a subroutine. The thick and dashed lines indicate the program flow for both of the CALL instructions. When the processor executes the CALL, it places the address of the next instruction (the return address) in the stack memory, and then passes control to the subroutine. The subroutine ends with a RETURN instruction which reads the return address from the stack and returns it to the main program at the point indicated. Each CALL instruction overwrites the return address of the previous CALL with its own return address. If a return address for a subroutine that is still active is already present in the stack memory, the new return address simply stacks up next to it and is read back in reverse order when the sub-routine is completed. A little thought will show that this allows a sub-routine to be nested within a subroutine, the stack providing the correct return paths and in the correct order. Fortunately, the microprocessor manages its stack memory automatically in conjunction with its stack pointer register.

SCOTTISH TECHNICAL EDUCATION COUNCIL

Certificate Course in Electrical and Electronic Engineering

The questions given below are from examination papers set by the Scottish Technical Education Council (SCOTEC) and are reproduced with the permission of the SCOTEC. The answers given have been prepared by independent authors. Sometimes, additional tutorial information is given; this is enclosed within square brackets to distinguish it from the information that would be expected of students under examination conditions. Answers to some questions are occasionally omitted because of insufficient space.

SCOTEC: TRANSMISSION SYSTEMS III 1983

Students were required to attempt all questions in Section A and four questions from Section B. Each question in Section A carried 5 marks, and each question in Section B carried a total of 25 marks. The time allowed was three hours

This test was set for students in Scotland studying under the British Telecom External Students Scheme (ESS). The ESS syllabus for Transmission Systems III follows the BTEC standard unit U81/741. This paper may therefore be of interest to BTEC students studying this unit.

SECTION A

Q1 An FSK system with a data transmission speed of 600 bit/s uses 1300 Hz and 1700 Hz as carrier frequencies; calculate the bandwidth required.

A1 The bandwidth, B, is given by

$$B = 2R + f_1 - f_2,$$

where R is the bit rate,
f_1 is the lowest carrier frequency, and
f_2 is the highest carrier frequency.
Substituting values into the expression gives,

$$B = 2 \times 600 + 1700 - 1300,$$

$$= \underline{1600\ \text{Hz}}.$$

Q2 List FIVE advantages which optical fibres have compared to metallic pairs.

A2 Any five from the following list of advantages:

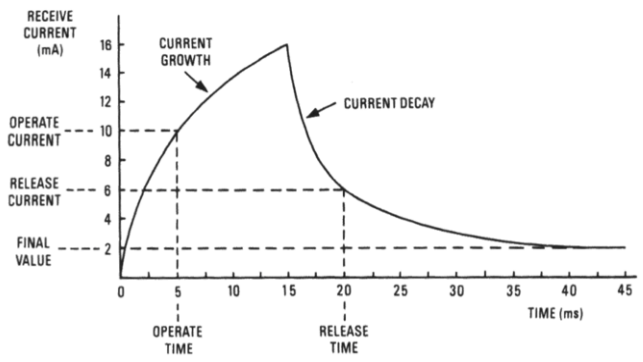
(*a*) wider bandwidth,
(*b*) lower raw-material costs,
(*c*) smaller cable diameter,
(*d*) negligible crosstalk between fibres,
(*e*) high immunity to external electrical interference, and
(*f*) greater spacing between regenerators.

Q3 Draw and label a typical line current curve, using the values listed, for a telegraph circuit using single-current working.

Final value = 2 mA.
Operate value = 10 mA.
Release value = 6 mA.

The curve should show the effects of growth and decay.

A3

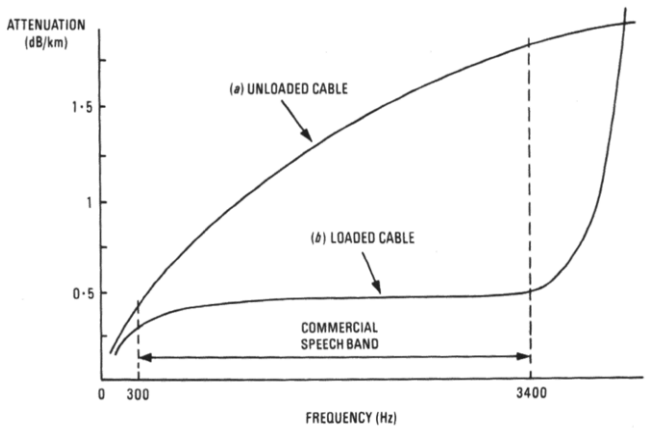


[*Tutorial note:* The values given are consistent with typical values in practice.]

Q4 Sketch a typical attenuation/frequency curve for a cable, operating over the commercial speech range when:

(*a*) *unloaded, and*
(*b*) *loaded.*

A4



Q5 Explain the advantages of voice-frequency signalling over DC signalling when long distances are involved.

A5 The advantages of voice-frequency (VF) signalling over DC signalling are:

(*a*) VF signals can be amplified by using standard telephony amplifiers; DC signals require regeneration equipment.
(*b*) VF signalling avoids the need to provide separate signalling paths and cables on existing transmission systems.
(*c*) The distance over which VF signals can be transmitted is the same as for normal telephone speech. Successive regeneration of DC signals increases the signal distortion to unacceptable levels, and the number of times a signal is regenerated limits the distance over which DC signals can be transmitted.

Q6 Explain briefly the limitations of single-current signalling.

A6 The limitations of single-current working are the resistance and capacitance of the transmission line. The resistance limits the amount of current available to operate the receive relay. The capacitance affects the rise and fall times of the line current and, hence, restricts the speed of working.

Q7 Calculate the bit rate of a 30-channel PCM system which has a sampling rate of 8 kHz and 256 binary codes.

A7 Bit rate = sampling frequency
× number of bits per word
× number of channels in the system,

= 8000 × 8 × 30 bit/s,

= 1·92 Mbit/s.

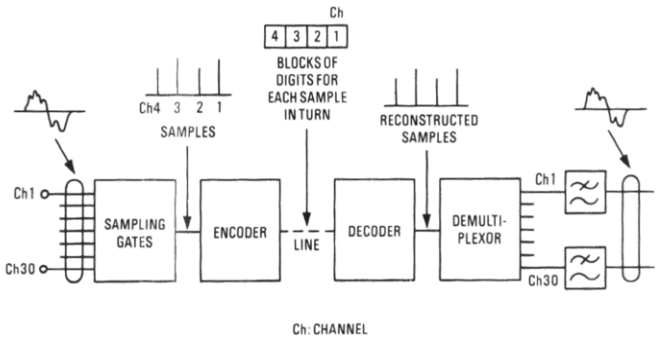
[*Tutorial note:* If a CCITT standard 30-channel pulse-code modulation system as used by British Telecom is assumed, in which two time-slots are used for signalling and synchronisation purposes, then an alternative answer would be:

bit rate = 8000 × 8 × 32 bit/s,

= 2·048 Mbit/s.]

Q8 By means of a suitable block diagram, show that arrangement of a simple PCM system; indicate the waveform at each stage.

A8



Ch: CHANNEL

Q9 Explain the need for synchronisation between transmitting and receiving stations in a PCM system.

A9 The transmitting and receiving stations of a pulse-code modulation system must be synchronised to ensure that information sent by one customer connected to a specific channel at the sending station is received by another customer connected to the same channel at the receiving station.

Q10 (*a*) *With reference to an optical-fibre transmission system:*

(*i*) *list* TWO *devices used as light sources, and*
(*ii*) *list* TWO *devices used as light detectors.*

(*b*) *State the range of wavelengths used by optical-fibre transmission systems.*

A10 (*a*) (*i*) The devices used as light sources in an optical-fibre transmission system are

(1) light-emitting diodes (LEDs), and
(2) lasers.

(*ii*) Two devices used as light detectors in an optical-fibre transmission system are

(1) p i n photodiodes, and
(2) avalanche photodiodes.

(*b*) The range of wavelengths used in optical-fibre transmission systems is from 800 nm to 1300 nm.

[*Tutorial note:* Within this range of wavelengths, there are three operating regions, called *windows*, which have low attenuations. It is these regions that are actually used for the transmission of information.]

SECTION B

Q11 (*a*) *Explain the following terms in relation to an optical-fibre:*

(*i*) *stepped index, and*
(*ii*) *graded index.*

(*b*) *Explain the following terms in relation to transmission of light through an optical fibre:*

(*i*) *monomode,*
(*ii*) *multimode.*

(*c*) *State the type of modulation used in optical-fibre transmission systems and describe how this is achieved.*

A11 (*a*) (*i*) The term *stepped index* is used to describe the type of optical fibre that has a distinct step in refractive index between the core and cladding.

(*ii*) The term *graded index* is used to describe the type of optical fibre whose refractive index changes gradually from the centre of the fibre to the outer boundary of the fibre.

(*b*) (*i*) The term *monomode* [or *singlemode*] is used to describe a fibre in which only one ray of light is transmitted.

(*ii*) The term *multimode* is used to describe a fibre in which several rays of light are transmitted.

(*c*) Direct modulation is used in optical-fibre transmission systems. It is achieved by using the ON/OFF action of a digital signal to switch a light source on and off. Demodulation of the light signal at the receiving station is achieved by a photodiode converting the ON/OFF light signals to ON/OFF electrical signals.

Q12 (*a*) *Explain, with the aid of sketches, the process of quantising and binary coding in a PCM system.*

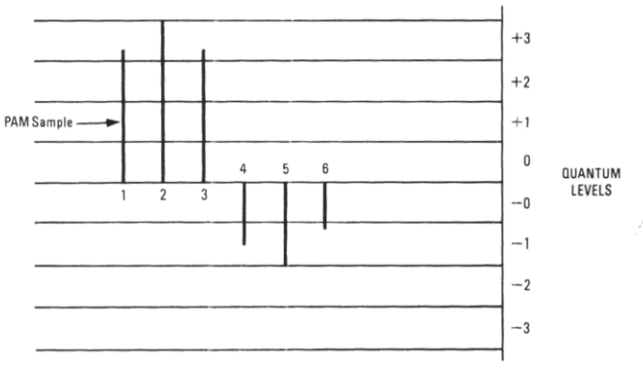
(*b*) *Explain the term 'quantisation noise' and outline how this can be minimised.*

(*c*) *Calculate the bit rate of a 30-channel PCM system that transmits 512 000 eight-bit words every 2 s.*

(*d*) *Explain the format of an 8-bit word in a 30-channel PCM system.*

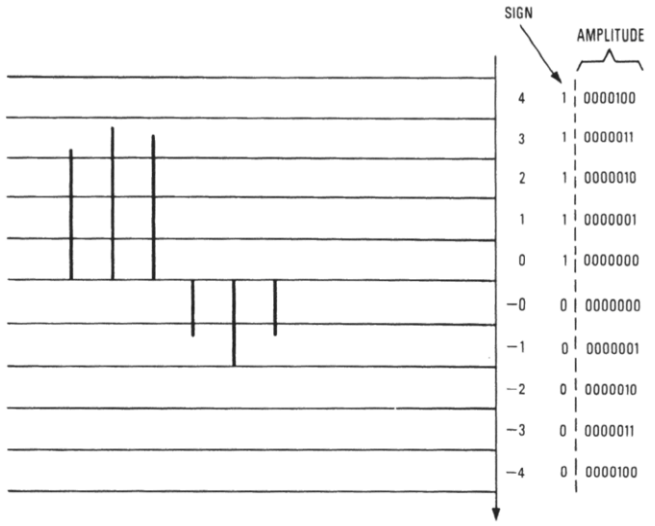
A12 (*a*) Quantising is a process by which a small range of amplitude variations are approximated to a single amplitude. Each range of amplitudes is called a *quantum level* and is represented by a sign and number.

Sketch (*a*) shows the amplitudes of six pulse-amplitude modulation (PAM) samples. Samples 1, 2 and 3 all lie within one quantum level. These samples are approximated to one value represented by the quantum level +3. Similarly, samples 4, 5 and 6 are approximated and represented by the quantum level −1.



(*a*)

The process of coding, which follows quantising, requires the allocation of binary codes to represent the quantum levels. In a typical 30-channel pulse-code modulation (PCM) system having 256 quantum levels, eight digits are needed. Seven of these eight digits are used to represent 128 amplitude levels above and below the middle of the quantum scale. An extra digit represents the sign (+ or −) of the quantum level. Sketch (*b*) shows a typical allocation of the binary digits to part of the quantum scale.



(*b*)

Samples 1, 2, and 3 are represented in sketch (*b*) by the binary code 1000 0011, and samples 4, 5 and 6 are represented by the code 0000 0011.

(*b*) The difference in amplitude between a reconstructed sample at the receiving end and the original sample at the transmitting end is called *quantising noise.*

Quantising noise occurs because the reconstructed sample has an amplitude equal to the midpoint of a quantum range, and the original sample can be at any amplitude within the range of the quantum level.

Quantising noise can be minimised by reducing the range of amplitude values covered by a quantum level.

(*c*) Bit rate $= \dfrac{\text{number of bits}}{\text{time}}$,

$= \dfrac{512\,000 \times 8}{2}$ bit/s,

$= \underline{2{\cdot}048\ \text{Mbit/s.}}$

(*d*) The 8 bit word in a 30-channel PCM system consists of seven bits that represent the amplitude of the samples and an eighth bit that represents the sign of the signal sample.

Q13 (*a*) *Name the four primary coefficients which can be used to represent the electrical characteristics of a cable pair.*

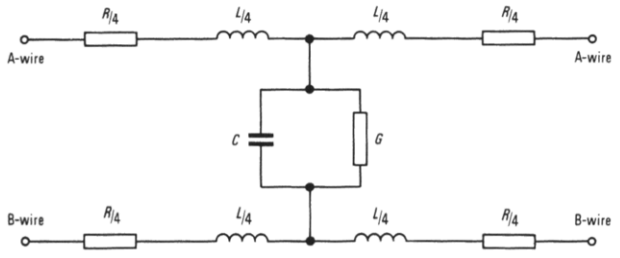
(*b*) *By means of a diagram, show how the distributed characteristics of a uniform transmission line can be represented in terms of lumped primary characteristics.*

(*c*) *Explain how the primary coefficients are affected by variation in signal frequency.*

A13 (*a*) The four primary coefficients used to represent the electrical characteristics are:

(*i*) resistance (R),
(*ii*) leakance or conductance (G),
(*iii*) capacitance (C), and
(*iv*) inductance (L).

(*b*)



(*c*) At very low frequencies, the resistance of a transmission line conductor is constant. Above about 10 kHz, the resistance increases as frequency (f) increases, and above 20 kHz the resistance increases according to the relation $R \propto \sqrt{f}$.

The leakage increases as frequency increases; above 30 kHz, the leakance increases according to the relation $G \propto f$.

The capacitance decreases only slightly with increase of frequency.

The inductance decreases with increasing frequency between 10 kHz and 20 kHz. Above 20 kHz, the inductance remains practically constant.

Q14 (*a*) *Explain, with the aid of sketches, the following terms:*

(*i*) *group delay, and*
(*ii*) *relative group delay.*

(*b*) *Sketch typical relative group delay/frequency curves for:*

(*i*) *unloaded cables,*
(*ii*) *loaded cables, and*
(*iii*) *coaxial cables.*

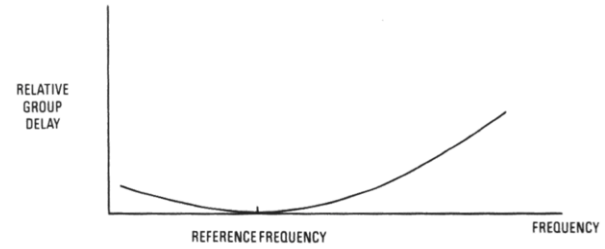
(*c*) *Explain the variation of group delay in audio unloaded cables, over the speech range 300 to 3400 Hz, in terms of the primary coefficients.*

(*d*) *Explain how 'group delay' affects transmission in analogue and digital systems.*

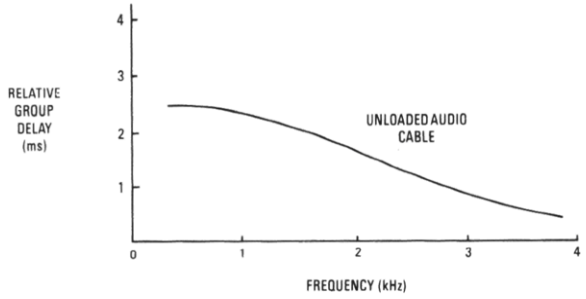
A14 (*a*) (*i*) Group delay is the propagation time between transmitter and receiver of a group of frequencies.

(*ii*) Relative group delay is the difference in propagation time between a frequency and a reference frequency.

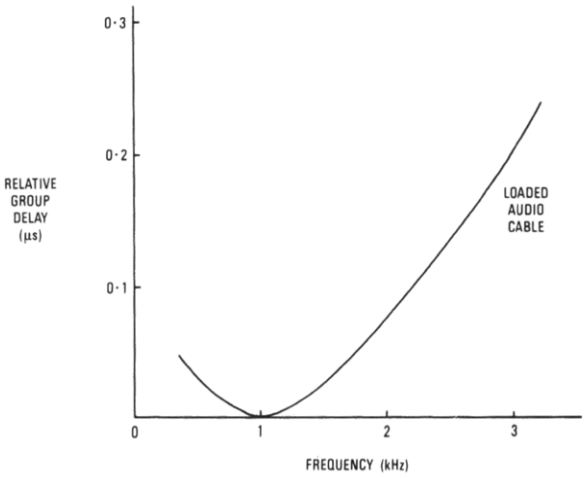
The sketch shows a typical graph of relative group delay against frequency.



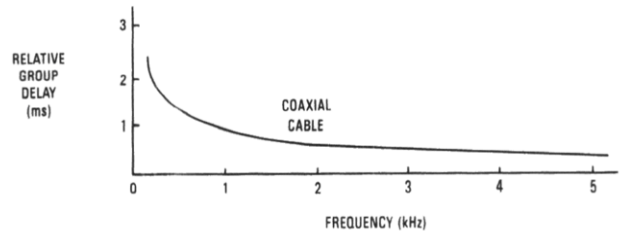
(*b*) (*i*)



(*ii*)



(*iii*)



(*c*) Over the speech band 300 to 3400 Hz, the group delay in audio unloaded cables varies in the following manner:

$$\text{group delay} \simeq \sqrt{\left(\frac{RC}{2\omega}\right)},$$

where ω is $2\pi \times$ frequency.

(*d*) Group delay in analogue systems, that is, those conveying speech or music, has little affect upon the signals. Group delay in digital systems causes the frequencies of pulse waveforms to arrive out of step and, thus, distort the pulse waveforms.

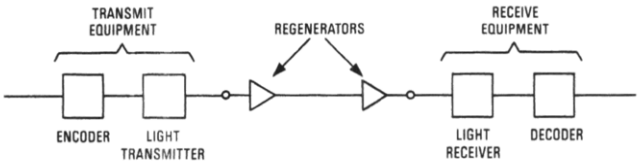
Q15 (*a*) *Sketch and label a simple block diagram of a unidirectional optical-fibre transmission system.*

(*b*) *With reference to an optical-fibre transmission system, explain the operation of:*

(*i*) *a digital transmitter, and*
(*ii*) *a digital receiver.*

(*c*) *Explain the need for regenerators.*

A15 (*a*) Sketch (*a*) shows a simple block diagram of a unidirectional optical-fibre transmission system.

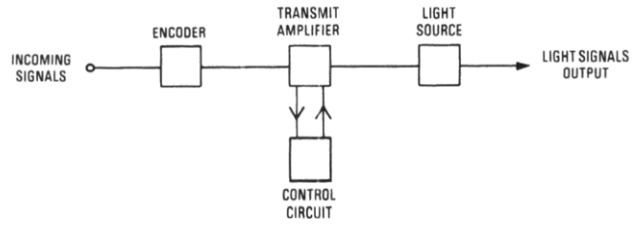


(*a*)

(*b*) (*i*) Sketch (*b*) shows the transmit equipment of an optical-fibre digital transmitter.

Operation

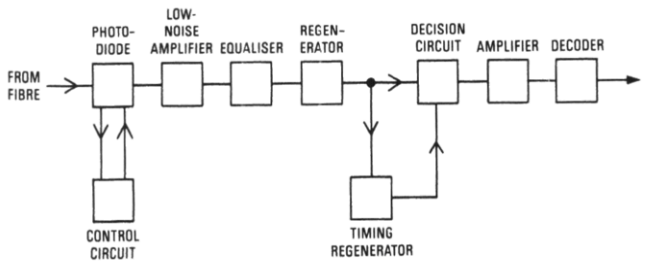
(1) Incoming digital signals are suitably coded by the encoder.
(2) The encoded signals are then amplified by the transmit amplifier to provide sufficient energy to drive the light source.
(3) The light source is modulated by the amplified digital signal.



(*b*)

(4) The control circuit, which includes a feedback arrangement, maintains the light source at a constant level, compensating for variations such as ageing and temperature fluctuations.

(*ii*) Sketch (*c*) shows a digital receiver of an optical-fibre transmission system.



(*c*)

Operation

(1) The photodiode detects the incoming light signals and converts them to electrical signals.
(2) The low-noise amplifier increases the strength of the electrical signals.
(3) The equaliser shapes the signals.
(4) The regenerator reforms the signal into square waves and extracts timing information.
(5) The decision circuit and timing regenerator form part of the signal timing.
(6) The amplifier increases the strength of the reformed signal.
(7) The decoder reconstitutes the signal into its original form.

(*c*) Regenerators are needed at intervals on some long optical-fibre routes to amplify and reform the signals.

Answers contributed by G. Wright

SCOTEC: MATHEMATICS IV 1983

Students were expected to attempt all five questions in Section A, and four questions from Section B. The time for this paper was three hours

SECTION A

Q1 *Differentiate with respect to x:*

(*a*) $y = \dfrac{1}{4x^2 - 2x}$;

(*b*) $y = \ln \cos x$; *and*

(*c*) $y = \sqrt{x} \tan x$.

(13 marks)

A1 (*a*)
$$y = \frac{1}{4x^2 - 2x} = (4x^2 - 2x)^{-1}.$$

$$\frac{dy}{dx} = -1 \times (8x - 2)(4x^2 - 2x)^{-2},$$

$$= \frac{2(1 - 4x)}{(2x)^2(2x - 1)^2},$$

$$= \underline{\frac{1 - 4x}{2x^2(2x - 1)^2}}.$$

(*b*) $y = \ln \cos x.$

Let $u = \cos x$, and $y = \ln u.$

Then, $\dfrac{du}{dx} = -\sin x$, and $\dfrac{dy}{du} = \dfrac{1}{u} = \dfrac{1}{\cos x}.$

$\therefore \quad \dfrac{dy}{dx} = \dfrac{dy}{du} \times \dfrac{du}{dx},$

$= \dfrac{-\sin x}{\cos x} = \underline{-\tan x.}$

(*c*) $y = \sqrt{x} \tan x.$

Let $u = \sqrt{x} = x^{1/2}$, and $v = \tan x.$

Then, $\dfrac{du}{dx} = \tfrac{1}{2}x^{-1/2}$, and $\dfrac{dv}{dx} = \sec^2 x.$

$\therefore \quad \dfrac{dy}{dx} = u\dfrac{dv}{dx} + v\dfrac{du}{dx},$

$= \underline{\sqrt{x}\sec^2 x + \dfrac{1}{2\sqrt{x}}\tan x.}$

Q2 *Express*

$$(2 + j)^2 + \frac{2 - j}{1 + j3}$$

in the form $a + jb$. *(6 marks)*

A2 $(2 + \mathrm{j})^2 + \dfrac{2 - \mathrm{j}}{1 + \mathrm{j}3} = 4 + \mathrm{j}4 + \mathrm{j}^2 + \dfrac{(2 - \mathrm{j})(1 - \mathrm{j}3)}{(1 + \mathrm{j}3)(1 - \mathrm{j}3)},$

$= 3 + \mathrm{j}4 + \dfrac{2 - \mathrm{j}7 + \mathrm{j}^2 3}{10},$

$= \underline{2{\cdot}9 + \mathrm{j}3{\cdot}3.}$

Q3 (*a*) *Obtain the integrals:*

(*i*) $\displaystyle\int x(2x - 1)(x - 3)\,dx$; *and*

(*ii*) $\displaystyle\int 4 \sin\left(\frac{\pi}{3} - 2x\right) dx.$

(*b*) *Evaluate to four significant figures:*

(*i*) $\displaystyle\int_0^1 \frac{4}{1 + 2x} - exp\,(2x)\,dx;$

(*ii*) $\displaystyle\int_{\pi/6}^{\pi/3} 2\,cos\left(4x + \frac{\pi}{3}\right) dx.$ *(19 marks)*

A3 (*a*) (*i*) $\displaystyle\int x(2x - 1)(x - 3)\,dx = \int (2x^3 - 7x^2 + 3x)\,dx,$

$= \underline{\dfrac{x^4}{2} - \tfrac{7}{3}x^3 + \tfrac{3}{2}x^2 + c.}$

(*ii*) $\displaystyle\int 4 \sin(\pi/3 - 2x)\,dx = \frac{4}{(-2)}\{-\cos(\pi/3 - 2x)\} + c,$

$= 2\cos(\pi/3 - 2x) + c,$

$= \underline{2\cos(2x - \pi/3) + c.}$

(*b*) (*i*) $\displaystyle\int_0^1 \frac{4}{1 + 2x} - \exp(2x)\,dx$

$= [2\ln(1 + 2x) - \tfrac{1}{2}\exp(2x)]_0^1,$

$= 2\ln 3 - \tfrac{1}{2}\exp(2) - 2\ln 1 + \tfrac{1}{2}\exp(0),$

$= \underline{-0{\cdot}9973.}$

(*ii*) $\displaystyle\int_{\pi/6}^{\pi/3} 2\cos(4x + \pi/3)\,dx = [\tfrac{1}{2}\sin(4x + \pi/3)]_{\pi/6}^{\pi/3},$

$= \tfrac{1}{2}\sin\left(\frac{5\pi}{3}\right) - \tfrac{1}{2}\sin(\pi),$

$= \underline{-0{\cdot}4330.}$

Q4 *By expressing the left-hand side of the following equation as a product of two trigonometric functions, solve for values of* θ *in the range* $0° \leqslant \theta \leqslant 180°$

$$cos\ 5\theta - cos\ 3\theta = -sin\ 4\theta. \qquad \textit{(8 marks)}$$

A4 Left-hand side of equation $= \cos 5\theta - \cos 3\theta,$

$= -2\sin\left(\dfrac{5\theta + 3\theta}{2}\right)\sin\left(\dfrac{5\theta - 3\theta}{2}\right),$

$= -2\sin 4\theta \sin\theta.$

Hence, $-2\sin 4\theta \sin\theta = -\sin 4\theta.$

$\therefore \quad 2\sin 4\theta \sin\theta - \sin 4\theta = 0$

$\therefore \quad \sin 4\theta\,(2\sin\theta - 1) = 0$

$\therefore \quad \sin 4\theta = 0 \quad \text{or} \quad \sin\theta = \tfrac{1}{2}.$

Hence, $4\theta = 0°, 180°, 360°, 540°, 720° \quad \text{or} \quad \theta = 30° \quad \text{or} \quad 150°.$

$\therefore \quad \underline{\theta = 0°, 30°, 45°, 90°, 135°, 150° \quad \text{or} \quad 180°.}$

Q5 *Given the matrix,*

$$A = \begin{pmatrix} 2 & 6 \\ -1 & -3 \end{pmatrix},$$

(*a*) *state the element* a_{12}*;*
(*b*) *state the order of matrix* A*;*
(*c*) *state the order of the matrix* A^2*; and*
(*d*) *state whether matrix* A *has an inverse matrix or not.*
(4 marks)

A5 (*a*) [*Tutorial note:* The element a_{12} is in the first row and the second column.]
$a_{12} = \underline{6.}$

(*b*) [*Tutorial note:* The order of a matrix with m rows and n columns is $m \times n$.]
The order of matrix A is $\underline{2 \times 2.}$

(*c*) The order of A^2 is $\underline{2 \times 2.}$

(*d*) There is no inverse matrix. A is a singular matrix since the determinant $(2(-3) - 6(-1)) = 0.$

SECTION B

Each question in this section carried a total of 25 marks.

Q6 (*a*) *Evaluate to four significant figures:*

(*i*) $\displaystyle\int_1^2 (2 - x)^3\,dx;$

(*ii*) $\displaystyle\int_0^{\pi/3} sin\ x\ cos\ x\,dx;$ *and*

(*iii*) $\displaystyle\int_1^2 \frac{3 - x^2}{x}\,dx.$

(*b*) (*i*) *Sketch the curves* $y = \sin\theta$ *and* $y = \sin^2\theta$ *on the same axes for* $0 \leqslant \theta \leqslant \pi$.

(*ii*) *Determine the values of* θ *where the curves intersect or touch each other.*

(*iii*) *Obtain by integration, the area enclosed between these curves. State this value to four decimal places.*

A6 (*a*) (*i*) $\displaystyle\int_1^2 (2-x)^3\,dx = \left[-\tfrac{1}{4}(2-x)^4\right]_1^2,$

$= 0 + \tfrac{1}{4},$

$= 0{\cdot}2500.$

(*ii*) $\displaystyle\int_0^{\pi/3} \sin x\cos x\,dx = \frac{1}{2}\int_0^{\pi/3} \sin 2x\,dx,$

$= -\tfrac{1}{4}[\cos 2x]_0^{\pi/3},$

$= -\frac{1}{4}\left[\cos\frac{2\pi}{3} - \cos 0\right],$

$= -\tfrac{1}{4}[-0{\cdot}5 - 1],$

$= 0{\cdot}3750.$

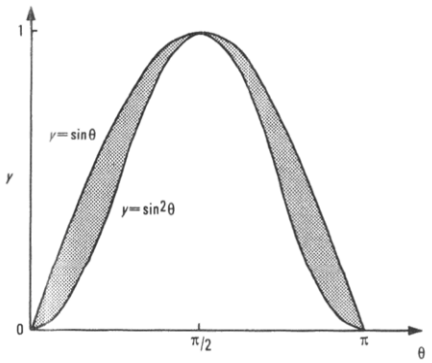
(*iii*) $\displaystyle\int_1^2 \frac{3-x^2}{x}\,dx = \int_1^2 \left(\frac{3}{x} - x\right)dx,$

$= \left[3\ln x - \frac{x^2}{2}\right]_1^2,$

$= 3\ln 2 - 2 - 3\ln 1 + \tfrac{1}{2},$

$= 0{\cdot}5794.$

(*b*) (*i*)



(*ii*) The curves intersect when $\sin\theta = \sin^2\theta$.

Hence, $\sin^2\theta - \sin\theta = 0.$

$\therefore \quad \sin\theta(\sin\theta - 1) = 0.$

$\therefore \quad \sin\theta = 0 \quad \text{or} \quad \sin\theta = 1.$

$\therefore \quad \theta = 0, \pi/2 \quad \text{or} \quad \pi.$

(*iii*) Area $= \displaystyle\int_0^{\pi} \sin\theta - \sin^2\theta\,d\theta,$

$= \displaystyle\int_0^{\pi} \sin\theta - \tfrac{1}{2}(1 - \cos 2\theta)\,d\theta,$

$= \displaystyle\int_0^{\pi} (\sin\theta - \tfrac{1}{2} + \tfrac{1}{2}\cos 2\theta)\,d\theta,$

$= \left[-\cos\theta - \frac{\theta}{2} + \frac{1}{4}\sin 2\theta\right]_0^{\pi},$

$= -\cos\pi - \frac{\pi}{2} + \frac{1}{4}\sin 2\pi + \cos 0 + 0 - \frac{1}{4}\sin 0,$

$= 0{\cdot}4292.$

Q7 The stepped wave shown in Fig. 1 has certain characteristics of the sine wave $i = I_m \sin\omega t$. *The maximum value of the stepped wave is* I_m *and* $k_1 > k_2$.

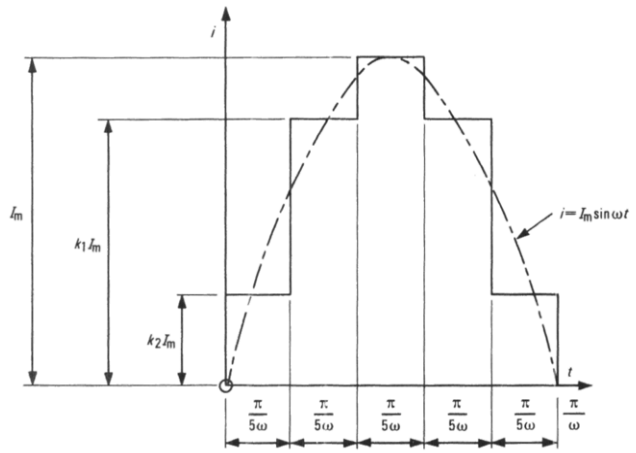


Fig. 1

(*a*) *Show that, when the stepped wave has the same mean value of* $(2/\pi)I_m$ *as the sine wave,*

$$k_1 + k_2 = \frac{5}{\pi} - \frac{1}{2} = 1{\cdot}0915.$$

(*b*) *Show that,*

$$k_1^2 + k_2^2 = 0{\cdot}7500$$

when the stepped wave has the root mean square value of

$$\frac{I_m}{\sqrt{2}}.$$

(*c*) *Solve the simultaneous equations*

$$k_1 + k_2 = 1{\cdot}0915$$
$$k_1^2 + k_2^2 = 0{\cdot}7500$$

State the values of k_1 *and* k_2 *to two decimal places.*

A7 (*a*) Mean value of stepped wave

$= \dfrac{\text{area under stepped wave}}{\text{base length of wave}},$

$= \dfrac{\frac{\pi}{5\omega}(I_m + 2k_1 I_m + 2k_2 I_m)}{\frac{\pi}{\omega}},$

$= \frac{2}{\pi} I_m$, as for sine wave.

Hence, $k_1 + k_2 = \frac{1}{2}\left(\frac{2}{\pi} \times 5 - 1\right),$

$= \frac{5}{\pi} - \frac{1}{2},$

$= 1{\cdot}0915.$ QED

(*b*) Mean of $i^2 = \left(\frac{I_m}{\sqrt{2}}\right)^2 = \frac{I_m^2}{2}$,

$$= \frac{\frac{\pi}{5\omega}(I_m^2 + 2k_1^2 I_m^2 + 2k_2^2 I_m^2)}{\frac{\pi}{\omega}}$$

Hence, $\frac{I_m^2}{2} = \frac{I_m^2}{5}(1 + 2k_1^2 + 2k_2^2)$,

and $k_1^2 + k_2^2 = \frac{1}{2}\left(\frac{5}{2} - 1\right)$,

$= \frac{3}{4}$,

$= 0{\cdot}7500.$ QED

(*c*) $k_1 + k_2 = 1{\cdot}0915$ ..... (1)

$k_1^2 + k_2^2 = 0{\cdot}7500$ ..... (2)

From equation (1), $k_1 = 1{\cdot}0915 - k_2$.

Substituting for k_1 in equation (2), gives

$$(1{\cdot}0915 - k_2)^2 + k_2^2 = 0{\cdot}7500.$$

$$\therefore \quad 2k_2^2 - 2{\cdot}1830k_2 + 0{\cdot}4414 = 0.$$

$$\therefore \quad k_2 = \frac{2{\cdot}1830 \pm \sqrt{(2{\cdot}1830^2 - 4 \times 2 \times 0{\cdot}4414)}}{2 \times 2},$$

$= 0{\cdot}2680$ or $0{\cdot}8235$.

When $k_2 = 0{\cdot}2680$, $k_1 = 1{\cdot}0915 - 0{\cdot}2680 = 0{\cdot}8235$,

and when $k_2 = 0{\cdot}8235$, $k_1 = 1{\cdot}0915 - 0{\cdot}8235 = 0{\cdot}2680$.

But $k_1 > k_2$; hence $k_1 = 0{\cdot}82$ and $k_2 = 0{\cdot}27$.

Q8 (*a*) (*i*) *Expand the function,*

$$y = 2\sin\left(\theta + \frac{\pi}{6}\right) + 3\cos\left(\theta - \frac{\pi}{3}\right).$$

(*ii*) *Express y in the form a sin θ + b cos θ.*
(*iii*) *Hence express y in the form R sin (θ + φ). Evaluate R and φ.*

(*b*) *Given that the complex number a + jb can be expressed by the matrix,*

$$\begin{pmatrix} a & -b \\ b & a \end{pmatrix}$$

(*i*) *Express the complex number, 4 − j3, in its matrix form.*
(*ii*) *Determine the inverse of this matrix.*
(*iii*) *Hence, by obtaining the product of two matrices, obtain the matrix representing the complex value*

$$\frac{3 + j}{4 - j3}.$$

A8 (*a*) (*i*) $y = 2\sin\left(\theta + \frac{\pi}{6}\right) + 3\cos\left(\theta + \frac{\pi}{3}\right)$.

$$= 2\sin\theta\cos\frac{\pi}{6} + 2\cos\theta\sin\frac{\pi}{6}$$

$$+ 3\cos\theta\cos\frac{\pi}{3} + 3\sin\theta\sin\frac{\pi}{3}.$$

(*ii*) $y = 2 \times \frac{\sqrt{3}}{2}\sin\theta + 2 \times \frac{1}{2}\cos\theta$

$$+ 3 \times \frac{1}{2}\cos\theta + \frac{3\sqrt{3}}{2}\sin\theta,$$

$$= \frac{5\sqrt{3}}{2}\sin\theta + \frac{5}{2}\cos\theta.$$ ..... (1)

(*iii*) Let $y = R\sin(\theta + \phi)$,

$= R\sin\theta\cos\phi + R\cos\theta\sin\phi$ ..... (2)

Equating the coefficients of sin θ, and then cos θ, in equations (1) and (2),

$$R\cos\phi = \frac{5\sqrt{3}}{2} \quad \text{and} \quad R\sin\phi = \frac{5}{2}.$$

$$\therefore \quad \frac{R\sin\phi}{R\cos\phi} = \tan\phi = \frac{1}{\sqrt{3}}.$$

$$\therefore \quad \phi = \frac{\pi}{6}.$$

[*Tutorial note:* φ is in the first quadrant since $R\cos\phi$ and $R\sin\phi$ are both positive.]

By squaring and adding,

$$(R\sin\phi)^2 + (R\cos\phi)^2 = R^2(\sin^2\phi + \cos^2\phi) = R^2.$$

Hence, $R^2 = \left(\frac{5}{2}\right)^2 + \left(\frac{5\sqrt{3}}{2}\right)^2 = 25.$

$R = 5.$

$\therefore \quad y = 5\sin(\theta + \pi/6).$

(*b*) (*i*) The matrix form of the complex number 4 − j3 is

$$\begin{pmatrix} 4 & 3 \\ -3 & 4 \end{pmatrix}.$$

(*ii*)

$$\begin{pmatrix} 4 & 3 \\ -3 & 4 \end{pmatrix}^{-1} = \frac{1}{4 \times 4 - (-3) \times 3}\begin{pmatrix} 4 & -3 \\ 3 & 4 \end{pmatrix},$$

$$= \frac{1}{25}\begin{pmatrix} 4 & -3 \\ 3 & 4 \end{pmatrix}.$$

(*iii*) The matrix form of $3 + j = \begin{pmatrix} 3 & -1 \\ 1 & 3 \end{pmatrix}$.

Hence $\frac{3 + j}{4 - j3} = \begin{pmatrix} 3 & -1 \\ 1 & 3 \end{pmatrix} \times \frac{1}{25}\begin{pmatrix} 4 & -3 \\ 3 & 4 \end{pmatrix}$,

$$= \frac{1}{25}\begin{pmatrix} 9 & -13 \\ 13 & 9 \end{pmatrix}.$$

Q9 (*a*) *Determine the location and nature of the stationary points on the curve*

$$y = x^2 + \frac{1}{x^2}.$$

(*b*) *An alternating current i is given by*

$$i = 4\sin 50\pi t + 2\sin 100\pi t,$$

where t is the time in seconds.

Find the smallest positive value of t which makes $\frac{di}{dt} = 0$.

Find also the corresponding value of i and the nature of this stationary value.

A9 (*a*)

$$y = x^2 + \frac{1}{x^2}.$$

At stationary points

$$\frac{dy}{dx} = 2x - \frac{2}{x^3} = 0.$$

Now, $$\frac{d^2y}{dx^2} = 2 + \frac{6}{x^4},$$

which is always positive; hence, minimum turning points are when $dy/dx = 0$.

At $\frac{dy}{dx} = 0$

$$x^4 = 1$$

$$\therefore \quad x = \pm 1$$

$$\therefore \quad y = (\pm 1)^2 + \frac{1}{(\pm 1)^2} = 2$$

Hence, the minimum turning points are at $\underline{(1,2)}$ and $\underline{(-1,2)}$.

(*b*)

$$i = 4 \sin 50\pi t + 2 \sin 100\pi t.$$

$$\frac{di}{dt} = 200\pi \cos 50\pi t + 200\pi \cos 100\pi t.$$

$$\frac{d^2i}{dt^2} = -10\,000\pi^2 \sin 50\pi t - 20\,000\pi^2 \sin 100\pi t.$$

At $\frac{di}{dt} = 0$,

$$200\pi \cos 50\pi t + 200\pi \cos 100\pi t = 0.$$

$$\therefore \quad \cos 50\pi t + \cos 100\pi t = 0.$$

[*Tutorial note:* $\cos(2 \times 50\pi t) = 2\cos^2 50\pi t - 1$.]

$$\therefore \quad 2\cos^2 50\pi t + \cos 50\pi t - 1 = 0.$$

$$\therefore \quad (2 \cos 50\pi t - 1)(\cos 50\pi t + 1) = 0.$$

$$\therefore \quad \cos 50\pi t = \tfrac{1}{2} \text{ or } -1.$$

$$\therefore \quad 50\pi t = \frac{\pi}{3}, \frac{5\pi}{3}, \pi.$$

Therefore, the smallest positive value of t when

$$\frac{di}{dt} = 0 \quad \text{is} \quad t = \underline{\tfrac{1}{150}\text{ s}}.$$

At $t = \frac{1}{150}$ s,

$$\frac{d^2i}{dt^2} = -10\,000\pi^2 \sin\frac{\pi}{3} - 20\,000\pi^2 \sin\frac{2\pi}{3},$$

$$= \text{negative value.}$$

Hence, this is a maximum turning point, and

$$i = 4 \sin\frac{\pi}{3} + 2 \sin\frac{2\pi}{3},$$

$$\underline{= 3\sqrt{3} = 5{\cdot}196.}$$

Q10 (*a*) *Differentiate with respect to x:*

(*i*) $y = \dfrac{\cos\left(3x + \dfrac{\pi}{4}\right)}{3\exp(x)}$; *and*

(*ii*) $y = \left(\dfrac{1 + 2x}{\sqrt{x}}\right)^3$.

(*b*) *Express in the form a + jb,*

$$\frac{4(\cos 2\theta + j \sin 2\theta)}{2(\cos\theta + j\sin\theta)} + (\cos 3\theta + j \sin 3\theta), \quad \text{where } \theta = \frac{\pi}{4}.$$

(*c*) *If* $\frac{1}{Z} = \frac{1}{r} + j\omega c + \frac{1}{j\omega L}$, *express Z in the form (a + jb).*

A10 (*a*) (*i*)

Let $$u = \cos\left(3x + \frac{\pi}{4}\right), \quad \text{and} \quad v = 3\exp(x).$$

Then, $$\frac{du}{dx} = -3\sin\left(3x + \frac{\pi}{4}\right), \quad \text{and} \quad \frac{dv}{dx} = 3\exp(x).$$

$$\frac{dy}{dx} = \frac{v\dfrac{du}{dx} - u\dfrac{dv}{dx}}{v^2},$$

$$= \frac{3\exp(x)\left\{-3\sin\left(3x + \dfrac{\pi}{4}\right)\right\} - \cos\left(3x + \dfrac{\pi}{4}\right) \times 3\exp(x)}{9\exp(2x)},$$

$$= \underline{\frac{-3\sin(3x + \pi/4) - \cos(3x + \pi/4)}{3\exp(x)}}$$

(*ii*) Let $u = x^{-1/2} + 2x^{1/2}$ and $y = u^3$.

$$\frac{du}{dx} = -\tfrac{1}{2}x^{-3/2} + x^{-1/2},$$

$$= \frac{-1}{2x\sqrt{x}} + \frac{1}{\sqrt{x}},$$

$$= \frac{(2x - 1)}{2x\sqrt{x}}.$$

$$\frac{dy}{du} = 3u^2,$$

$$= 3(x^{-1/2} + 2x^{1/2})^2,$$

$$= 3\frac{(1 + 2x)^2}{x}.$$

Now, $$\frac{dy}{dx} = \frac{dy}{du} \times \frac{du}{dx},$$

$$= \underline{\frac{3(2x - 1)(2x + 1)^2}{2x^2\sqrt{x}}}.$$

(*b*) At $\theta = \dfrac{\pi}{4}$,

$$\frac{4(\cos 2\theta + j \sin 2\theta)}{2(\cos\theta + j\sin\theta)} + (\cos 3\theta + j \sin 3\theta)$$

$$= \tfrac{4}{2}\{\cos(2\theta - \theta) + j \sin(2\theta - \theta)\} + (\cos 3\theta + j\sin 3\theta),$$

$$= 2\cos\frac{\pi}{4} + j2\sin\frac{\pi}{4} + \cos\frac{3\pi}{4} + j\sin\frac{3\pi}{4},$$

$$= \frac{1}{\sqrt{2}} + j\frac{3}{\sqrt{2}},$$

$$\underline{= 0{\cdot}7071 + j2{\cdot}1213.}$$

(*c*) $$\frac{1}{Z} = \frac{1}{r} + j\omega c + \frac{1}{j\omega L},$$

$$= \frac{1}{r} + j\omega c - \frac{j\omega L}{\omega^2 L^2},$$

$$= \frac{1}{r} + j\left(\omega c - \frac{1}{\omega L}\right),$$

$$= \frac{1}{r} + j\frac{(\omega^2 cL - 1)}{\omega L},$$

$$= \frac{\omega L + jr(\omega^2 cL - 1)}{\omega rL}.$$

$$\therefore \quad Z = \frac{\omega rL}{\omega L + jr(\omega^2 cL - 1)},$$

$$= \frac{\omega rL\{\omega L - jr(\omega^2 cL - 1)\}}{\{\omega L + jr(\omega^2 cL - 1)\}\{\omega L - jr(\omega^2 cL - 1)\}},$$

$$= \frac{\omega^2 L^2 r}{\omega^2 L^2 + r^2(\omega^2 cL - 1)^2} - j\frac{\omega r^2 L(\omega^2 cL - 1)}{\omega^2 L^2 + r^2(\omega^2 cL - 1)^2}.$$

Q11 (*a*) *Prove the identity*

$$\frac{\sin A + \sin 3A + \sin 5A}{\cos A + \cos 3A + \cos 5A} = \tan 3A.$$

(*b*) *A modulated voltage is expressed as*

$$v = (A + B \sin 50\pi t) \sin 100\pi t.$$

(*i*) *Show that*

$$v = A \sin 100\pi t + \frac{B}{2}\cos 50\pi t - \frac{B}{2}\cos 150\pi t.$$

(*ii*) *Hence, determine the mean voltage over the interval* $t = 0$ *to* $t = 0{\cdot}01$ *in terms of* A *and* B.

A11 (*a*) The left-hand side of the equation

$$= \frac{\sin 5A + \sin A + \sin 3A}{\cos 5A + \cos A + \cos 3A},$$

$$= \frac{2 \sin 3A \cos 2A + \sin 3A}{2 \cos 3A \cos 2A + \cos 3A},$$

$$= \frac{\sin 3A\,(2 \cos 2A + 1)}{\cos 3A\,(2 \cos 2A + 1)},$$

$$= \tan 3A.$$ QED

(*b*) (*i*) $v = (A + B \sin 50\pi t) \sin 100\pi t,$

$$= A \sin 100\pi t + B \sin 100\pi t \sin 50\pi t,$$

$$= A \sin 100\pi t + \frac{B}{2}\cos 50\pi t - \frac{B}{2}\cos 150\pi t.$$ QED

(*ii*) Mean voltage

$$= \frac{1}{0{\cdot}01 - 0}\int_0^{0{\cdot}01} v\,dt,$$

$$= 100\int_0^{0{\cdot}01}\left(A \sin 100\pi t + \frac{B}{2}\cos 50\pi t - \frac{B}{2}\cos 150\pi t\right)dt,$$

$$= 100\left[-\frac{A}{100\pi}\cos 100\pi t + \frac{B}{100\pi}\sin 50\pi t - \frac{B}{300\pi}\sin 150\pi t\right]_0^{0{\cdot}01},$$

$$= -\frac{A}{\pi}\cos\pi + \frac{B}{\pi}\sin\frac{\pi}{2} - \frac{B}{3\pi}\sin\frac{3\pi}{2} + \frac{A}{\pi}\cos 0 - 0 + 0,$$

$$= \frac{A}{\pi} + \frac{B}{\pi} + \frac{B}{3\pi} + \frac{A}{\pi},$$

$$= \frac{6A + 4B}{3\pi},$$

$$= 0{\cdot}6366A + 0{\cdot}4244B.$$

Answers contributed by A. Niven

BACK NUMBERS

The price of back numbers of the *Journal* is £1.50 each (51p to staff of British Telecom and the British Post Office), including the Supplement and postage and packaging. (The *Supplement* is not sold separately.)

BTEC AND SCOTEC: GUIDANCE FOR STUDENTS

Details of back issues of the *Journal* with *Supplements* containing question/answer material for students following the syllabi of the Business and Technician Education Council and the Scottish Technical Education Council courses for telecommunications technicians are given below.

BTEC Units

Digital Techniques II	Apr. 1983, Apr. 1984
Digital Techniques A III	Oct. 1983, July 1984
Electrical and Electronic Principles II	July 1983, Apr. 1984
Electrical and Electronic Principles III	Oct. 1983
Electrical Principles II	Jan. 1980, Jan. 1981, July 1982
Electronics II	Oct. 1980
Electronics III	July 1983, Apr. 1984
Line and Customer Apparatus I	Jan. 1979, July 1981, Apr. 1982, Apr. 1983, Apr. 1984
Lines II	Apr. 1981, Oct. 1982, Apr. 1984
Lines III	July 1983
Mathematics I	Jan. 1979, Apr. 1980
Mathematics II	Apr. 1980, Apr. 1982, July 1983, Apr. 1984
Micro-Electronic Systems I	July 1983, Apr. 1984
Micro-Electronic Systems II	Oct. 1983, July 1984
Physical Science I	Jan. 1979, Jan. 1980, July 1981
Radio II	Jan. 1983, Jan. 1984
Telecommunication Systems I	Jan. 1979, Jan. 1980, July 1981, July 1982, July 1983, Jan. 1984
Telephone Switching Systems II	Jan. 1980, Oct. 1982, Oct. 1983, July 1984
Telephone Switching Systems III	Jan. 1983
Transmission Systems II	July 1980, Jan. 1982, Jan. 1983, Jan. 1984
Transmission Systems III	Apr. 1983

SCOTEC Subjects

Introduction to Telecommunications Systems	Jan. 1979, Apr. 1982*
Digital Techniques and Transmission	July 1982*, Jan. 1984*
Electrical and Engineering Principles	Jan. 1979
Electrical Principles II	Jan. 1983
Electrical Principles III	July 1982*, July 1983*, July 1984*
Electronics III	Oct. 1982*
Mathematics I/II	Jan. 1979
Mathematics III	July 1982*, Apr. 1983*
Radio III	Oct. 1982*, Jan. 1984*
Switching Systems III	Apr. 1982*, July 1983*
Telecommunication Transmission Systems V	July 1984*

*Model answers to examinations set by SCOTEC.

EDUCATIONAL PAPERS PUBLISHED IN THE SUPPLEMENT

Field-Effect Transistors	Oct. 1982

MODEL ANSWERS TO CITY AND GUILDS OF LONDON INSTITUTE EXAMINATIONS

Details of back numbers of the *Journal* with *Supplements* containing model answers to past examinations of the City and Guilds of London Institute Telecommunication Technician's Course (old scheme) are given below.

Basic Microwave Communication C	Oct. 1978, July 1979, July 1980, Apr. 1981, Apr. 1982
Communication Radio C	Apr. 1978
Computers A	Apr. 1978, Apr. 1979, Apr. 1980
Computers B	Apr. 1978, July 1979, Apr. 1980, Apr. 1981
Elementary Telecommunication Practice	Apr. 1978, July 1979
Engineering Science	Apr. 1978
Line Plant Practice A	Apr. 1978, Apr. 1979, Apr. 1980
Line Plant Practice B	Oct. 1978, Jan. 1981, Apr. 1981
Line Plant Practice C	Oct. 1978, Jan. 1981, July 1981, Apr. 1982
Line Transmission C	Oct. 1978, Oct. 1979, Oct. 1980, Apr. 1981, Apr. 1982
Mathematics A	Apr. 1978, Apr. 1979, Jan. 1980
Mathematics B	Apr. 1978, Apr. 1979, Apr. 1980, Jan. 1981
Mathematics C	July 1978, Oct. 1979, July 1980, Apr. 1981, Jan. 1982
Practical Mathematics	Apr. 1979
Radio and Line Transmission A	Apr. 1979, Jan. 1980
Radio and Line Transmission B	Apr. 1978, July 1978
Telecommunication Principles A	Apr. 1978, Apr. 1979, Apr. 1980
Telecommunication Principles B	Oct. 1978, Apr. 1979, Apr. 1980, Jan. 1981
Telecommunication Principles C	Oct. 1978, Oct. 1979, Jan. 1980, Jan. 1981, Apr. 1982
Telegraphy B	Oct. 1978, Oct. 1979, July 1980, Jan. 1981
Telegraphy C	Oct. 1978, July 1979, Apr. 1980, Jan. 1981, Jan./Apr. 1982
Telephony and Telegraphy A	July 1978, Jan. 1980, Oct. 1980
Telephony B	July 1978, Jan. 1980, Oct. 1980
Telephony C	Oct. 1978, Apr. 1979, July 1980, Jan. 1981, Jan. 1982

The January and April 1982 back issues are no longer available.

Orders for back numbers of the *Journal*, by post only, should be addressed to *British Telecommunications Engineering Journal* (Sales), Post Room, 2–12 Gresham Street, London EC2V 7AG. Cheques and postal orders, payable to *'BTE Journal'*, should be crossed '& Co.', and enclosed with the order. Cash should not be sent through the post.

Published by *British Telecommunications Engineering Journal*, 2–12 Gresham Street, London EC2V 7AG
and printed in Great Britain by Unwin Brothers Limited, Old Woking, Surrey.